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Influence of spacer on symmetrical stepped InGaAs/InP DGMOSFET for enhancement of the device performance.

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ABSTRACT--*In this work the impact of spacer in InGaAs/InP hetero stepped double gate MOS transistor is investigated by a 2D TCAD device simulator. To minimize the short channel effects (SCEs), underlap technique is used symmetrically in either side of the gate. However, it considerably decreases the On current due to enhanced channel resistance. Thus the spacers on underlap region are one of the solutions to overwhelm these problems. Therefore, difficulties associated with conventional underlap DG MOSFET can be eliminated with significant improvement in On current and intrinsic gain. Further, to reduce the punch-through effect, stepped gate concept is integrated in the double gate MOSFET to attain a better control on the channel carriers that eventually reduces the leakage current. So this paper presents a comparison made between symmetric spacer underlap hetero stepped double gate (SSUHS-DG) MOSFET and hetero stepped double gate (HS-DG) MOSFET; so far SSUHS-DG MOSFET offers better device performance.*

Keywords*--Spacer, Short channel effect ,InGa$_0$As/InP,On resistance, stepped gate.*

I. INTRODUCTION

The advancement of CMOS technology demands the devices with low power dissipation, which needs the device dimension in nano-meter scale [1]. Therefore the short channel effects (SCEs) are more noticeable in scaled devices [2]. Investigation on novel and different MOS architecture has become very important to satisfy the above requirement. Nano scale multi-gate MOS structures are suitable for suppressing the short channel effects (SCEs) where DGMOSFET is one of those for enhancing the subthreshold performances.

The compound semiconductors mainly group III-V materials are very prevalent for its superior thermal conductivity, high saturation velocity and mobility [4-5]. The most desired hetero structure offers large CBO/VBO, which affords a necessary obstruction at the middle of the narrow-band channel, thus supports the carriers to restrict inside the channel [7]. However, $In_{0.53}Ga_{0.47}As$/InP is the most usable III-V material for its outstanding mobility and saturation velocity [8-11].

In a scaled device, decrease in gate length provides more impact of drain bias resulting in drain induced barrier lowering (DIBL) [12].Thus underlap technique is considered to decrease the effect of the drain bias on the device performance. This technique also provides the protection against the fringing capacitance and the drain leakage

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[13-14]. But due to increased effective channel resistance, the double gate (DG) MOSFETs with underlap reduces the On current (I_{on}) [15-19].Thus for enhancement of the I_{on}, the use of spacer with underlap in conventional DG devices decrease the divergence of the fringing fields at underlap region and resulting in improved analog performances [20].

Further, the substrate doping concentration beyond $1x10^{17}cm^{-3}$ provides more parasitic capacitance and junction leakage [21-23]. Therefor a stepped gate MOSFET can achieve a better control upon the carriers in the channel region and the leakage current also reduces due to lower junction capacitance.Further, asymmetric oxide thickness in gate region delivers higher transconductance, lower power dissipation and switching delays for which MOSFET with stepped gate is suitable for low power and high speed solicitations [24].

In this work the effect of spacer on the electrostatic performance of SSUHS-DG MOSFET has been analyzed. The objective of this work is to compare the analog performance of proposed device with HS-DG MOSFET in order to validate SSUHS-DG MOSFET with respect to On current, threshold voltage and switching ratio. All the device characteristics have been achieved using 2D TCAD platform and SSUHS-DG MOSFET gives better performance as compared to HS-DG MOSFET.

II. 2DEVICE STRUCTURALDESCRIPTIONS:

The schematic of HS-DG MOSFET and SSUHS-DG MOSFET are shown in Fig.1. (a) and (b) respectively [25]. In the suggested structure the channel region consists of InGaAs/InP material and three stepped gate with increased oxide thickness from source side to drain side. Further for performance enhancement a symmetrical spacer material air, in either side of the gate is introduced in the proposed device. The drain and source extension of proposed structure is 15nm each with doping profile of$N_D = 10^{20}\, cm^{-3}$. The work function of the gate material is considered as 5.1eV. Two wideband InP barrier layers are implanted in either side of the undoped narrow band $In_{0.53}Ga_{0.47}As$ channel. The device specification are listed in table I .

Table 1: The device dimensional specification:

Device Parameters	**Stepped gate with spacer device**
t_1	0.25nm
t_2	0.5nm
t_3	1.5nm
L_{g1}	4nm
L_{g2}	7nm
L_{g3}	4nm
L_{sp}	10nm
Channel length(L_g)	15nm

Narrow band layer thickness	3nm
Wide band layer thickness	3nm

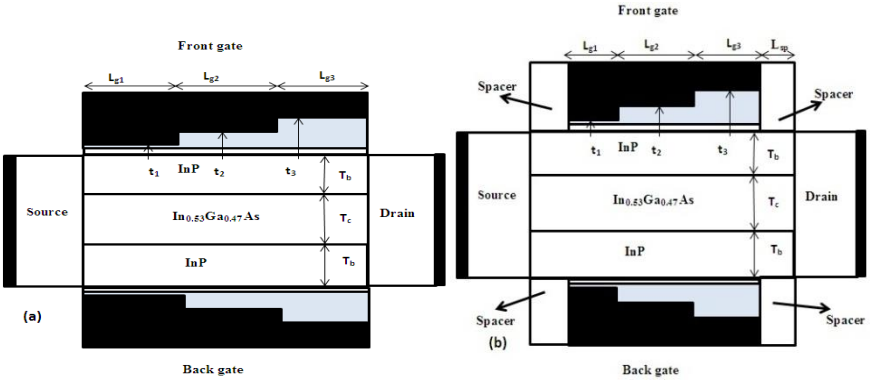

Figure 1: Schematic structures of (a) HS-DG MOSFETand (b) SSUHS-DG MOSFET.

III. RESULTS DISCUSSION

The variation of transfer characteristics and transconductance (g_m) against gate voltage for SSUHS-DG MOSFET and HS-DG MOSFET at $V_{ds} = 1.0\,V$illustrates in fig 2 (a) and (b). From the figure it is shown that, SSUS-DG MOSFET gives better On current and higher transconductance as compared to HS-DG MOSFET. In fact the introduction of symmetrical spacer near the gate region supports to extra charge carrier in the channel. This further helps to improve the current and transconductance.

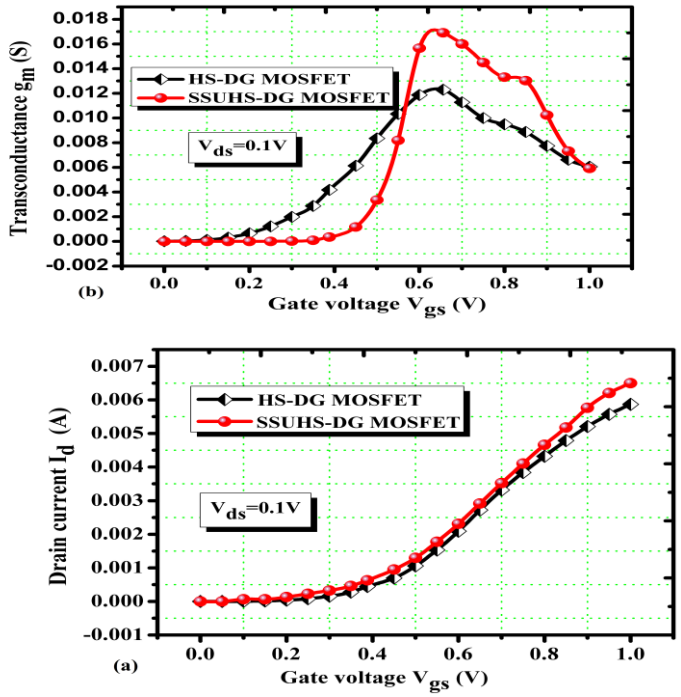

Figure 2: Variation (a) drain current and (b) trasconductance with gate voltage for V_{ds} =0.1 V

The drain characteristic and conductance (g_{ds}) against drain voltage for SSUHS-DG MOSFET and HS-DG MOSFET at $V_{gs} = 1.0\,V$ is shown in figure 3 (a) and (b). From the analysis it is interpreted that SSUHS-DG MOSFET gives better output current and lower output conductance due shorter channel length, which enforces the carriers to transporting along the channel with a high speed. The proposed device exhibits low peak electric field at the drain end, which ensures that the device gives lower output conductance.

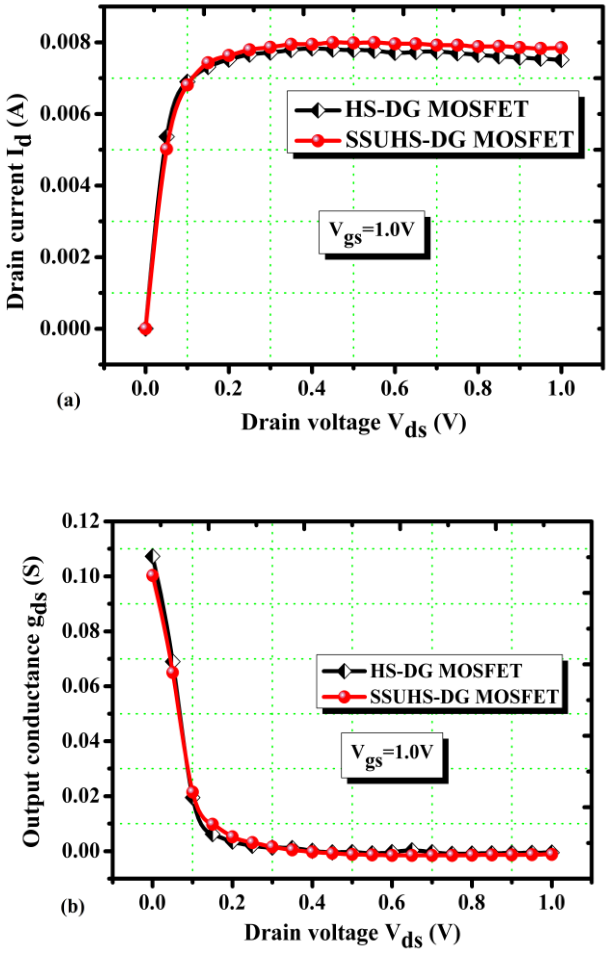

Figure 3 : Variation of (a) drain current and (b) output conductance with drain voltage for $V_{gs} = 1.0\,V$.

The variation of threshold voltage and switching ratio with respect to gate voltage for the two devices at constant $V_{ds} = 0.5\,V$ is shown in fig. 4 (a) and (b). From the graph it is noticeable that the threshold voltage reduces with increase in gate voltage and it is due to the impact of spacer in HS-DG MOSFET. Again in case of proposed device, switching ratio increases with increase in gate voltage. Switching ratio is the essential constraint in CMOS technology. The device gives larger switching ratio means it has lower static power dissipation.

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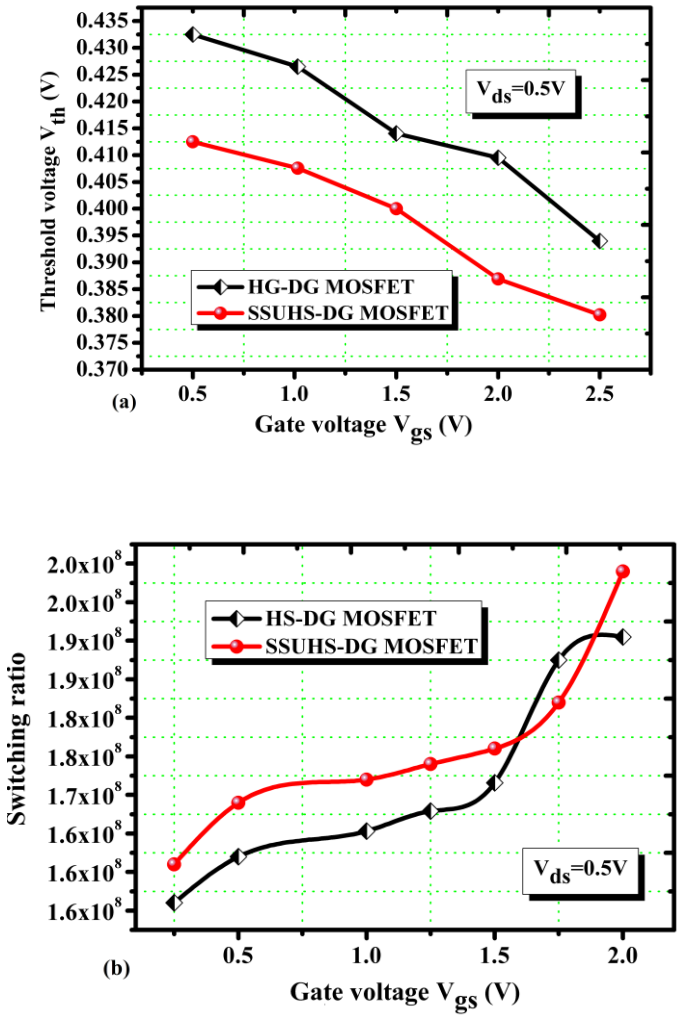

Figure 4: Variation of (a) threshold voltage and (b) switching voltage with gate voltage for $V_{gs} = 1.0\,V$.

IV. CONCLUSION

This work introduce an air spacer in symmetrical underlap HS-DG MOSFET to establish SSUHS-DG MOSFET. The device characteristics are inspected through 2-D TCAD simulator and comparisons are made with SSUHS-DG MOSFET and HS-DG MOSFET. The simulation upshots of SSUHS-DG MOSFET provides a better characteristics with respect to On current, threshold voltage and switching ratio against HS-DG MOSFET thus appropriate for faster switching operation.

REFERENCE

1. International Technology Roadmap for Semiconductor, 2012.
2. Xie, Q., Xu, J., Taur, Y. : Review and critique of analytic models of MOSFET short-channel effects in subthreshold regime,Vol.59. IEEE Trans. Electron Devices. (2012) 1569e1579.
3. Taur, Y., Ning, T.H.: Fundamentals of Modern VLSI Devices, Cambridge university press, 2009.

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4. Robert, C., Doyle, B., Suman, D.: Integratednanoelectronicsfor the future, Vol.6.Nat Mater, (2007) 810–820.
5. Sarkar, A., Jana, R.: The influence of gate underlap on analog and RF performance of III–V heterostructure double gate MOSFET, Vol.73. Superlattices and Microstructures. (2014) 256–267.
6. Chau, R., Datta, S., Majumdar, A.: Opportunities and Challenges of III-V Nanoelectronics for Future High-Speed, Low-Power Logic Applications Compound Semiconductor Integrated Circuit Symposium,(2005) Palm Springs, CA,.
7. Pati, S. K. et.al.: Impact of gate length and barrier thickness on the performance of InP/InGaAs Based Double Gate Metal-OxideSemiconductorHeterostructure Field- Effect Transistor (DG MOSHFET),Vol.55. Superlattices and Microstructures. (2013) 124001-6.
8. Lau, K. M., Tang, C. W., Li, H. O., Zhong, Z. Y.: AlInAs/GaInAsmHEMTs on silicon substrates grown by MOCVD in IEDM Tech. Dig., (2008) 1–4.
9. Oktyabrsky, S., Peide, D.Y.: Fundamentals of III–V Semiconductor MOSFETs. Springer, New York, 2010.
10. Egard, M., Ohlsson, L., Borg, B. M., Lenrick, F., Wallenberg, R., Wernersson, L.E., Lind, E.: High transconductance self-aligned gate-last surface channel In0.53Ga0.47As MOSFET in IEDM Tech. Dig., (2011), 13.2.1–13.2.4.
11. Radosavljevic,M., Dewey, G., Fastenau, J.M., Kavalieros, J., Kotlyar, R., Chu-Kung, B., Liu, W.K., Lubyshev, D., Metz, M., Millard, K., Mukherjee, N., Pan, L.,
12. Pillarisetty, R., Rachmady, W., Shah, U., Chau, R.: Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-toSource Separation for Low Power Logic Applications in Proc. IEDM Tech. Dig. (2010) 6.1.1–6.1.4.
13. Paul, B.C., Bansal, A., Roy, K.: Underlap DGMOS for digital-sub threshold operation,Vol.53. IEEE Trans. Electron Device (2006) 910e913.
14. A.B. Sachid, C.R. Manoj, D.K. Sharma, V.R. Rao, Gate fringe-induced barrier lowering in underlapFinFET structures and its optimization,Vol.29. IEEE Electron Device Lett. (2008) 128e130.
15. Bansal, A., Paul, B.C., Roy,K.: Modeling and optimization of fringe capacitance of nanoscale DGMOS devices, Vol.52.IEEE Trans. Electron Devices .(2005) 256e262.
16. Fossum, J.G., Chowdhury, M.M., Trivedi, V.P., King, T.J., Choi, Y.K., An,J., Yu, B.: Physical insights on design and modeling of nanoscaleFinFETs, IEEE Int. Electron Devices Meeting Tech. Dig. (2003) 29.1.1e29.1.4.
17. Kilchytska, V., eve, A., Vancaillie, N_ L., Levacq, D., Adriaensen, S., VanMeer, H.: Influence of device engineering on the analog and RF performance of SOI MOSFETs,Vol.52. IEEE Trans. Electron Devices .(2003) 577e588.
18. Trivedi,V.P., Fossum, J.G., Chowdhury, M.M.: NanoscaleFinFETs with gateesource/drain underlap,Vol.52. IEEE Trans. Electron Devices .(2005) 56e62.
19. Liang, X., Taur, Y.: A 2-D analytical solution for SCEs in DG MOSFETs, Vol.51.IEEE Trans. Electron Devices .(2004) 1385e1391.
20. Sarkar,A., Jana, R.: The influence of gate underlap on analogandRF performance of IIIeVheterostructure double gate MOSFET,Vol.73.Superlattices Microstruct.(2014) 256e267.

21. Kundu, A., Koley, K., Dutta, A., Sarkar, C.K.: Impact of gate metal work-function engineering for enhancement of subthresholdanalog/RF performance of underlap dual material gate DG-FET,Vol.54. Microelectron. Rel. (2014) 2717e2722.
22. Sachid, A.B., Francis, R., Baghini, M.S., Sharma, D.K., Bach, K.H., Mahnkopf, R., RamgopalRao, V.: Sub-20 nm gate length FinFET design: can high-k spacers make a difference IEDM Tech. Dig. (2008)1e4.
23. Rodder, M., Aur, S., Chen, I. -C.: A Scaled 1.8 V, 0.18 pm Gate Length CMOS Technology: Device Design and Reliability Considerations, IEDM Tech. Dig. (1995) pp. 415-418.
24. Chatterjee, A., Liu, J., Aur, S., Mozumder, P. K., Rodder, M., Chen, I.-C.: Pass Transistor Designs using Pocket Implant to Improve Manufacturability for 256 Mbit DRAM and Beyond, IEDM Tech. Dig. 1994, pp. 87-90.
25. Saxena, R. S.: A Stepped Oxide Hetero-Material Gate Trench Power MOSFET for Improved Performance.Vol. IEEE Transactions on Electron Devices, (2009).
26. Atlas User's Manual: Device Simulation Software, SILVACO Int. 2010.
27. PHADE, GAYATRI, and BK MISHRA. "RF PERFORMANCE AND MODELLING OF OPTICALLY CONTROLLED MOSFET." International Journal of Electronics and Communication Engineering (IJECE) 2.2 (2013): 57-64
28. JAIN, PRAMOD, DS AJNAR, and PANKAJ NAIK. "A CMOS TRANSCONDUCTOR WITH ENHANCED LINEARITY AND TUNABILITY IN 0.18 µm TECHNOLOGY."International Journal of Electronics and Communication Engineering (IJECE) 2.4 (2013): 175-182
29. ARORA, NEHA, et al. "High gain and phase margin cmos operational amplifier designs International Journal of Electrical and Electronics Engineering Research (IJEEER) 3.2 (2013): 19-28.
30. PANDA, SARADINDU, et al. "Comparative study of thermal noise of Si surrounding gate MOSFET (SGMOSFET) with different gate oxides." *International Journal of Semiconductor Science & Technology (IJSST)* 3.2 (2013): 17-22.
31. CHANG, FANG-WEI, JYH-LING LIN, and YOUNG-HUANG CHOU. "STUDY OF 600 V-CLASS SUPERJUNCTION METAL–OXIDE–SEMICONDUCTOR FIELD-EFFECT TRANSISTORS WITH TERMINATION OF TRENCH STRUCTURE AND SIPOS."International Journal of Electrical and Electronics Engineering Research (IJEEER) 6.6 (2016): 13-24
32. CHAKROBORTY, ANINDYA SHUBRO, and JAVED HOSSAIN. "PERFORMANCE COMPARISON OF ELECTRICAL PARAMETERS BETWEEN GANFINFET AND SI-FINFET NANO DEVICES."International Journal of Semiconductor Science & Technology (IJSST) 9.1 (2019): 1-12
33. Saha, Nandini, et al. "Comparative Study of IV-Characteristics of PIN Diode at Different Doping Concentrations for Different Semiconductor Materials Using TCAD." *International Journal of Electronics and Communication Engineering (IJECE)* 4.6 (2015): 1-8.
34. KUMAR, VINOD, and RS GAMAD. "DESIGN OF RING OSCILLATOR USING CS-CMOS FOR MIXED SIGNAL SOCS."International Journal of Electrical and Electronics Engineering (IJEEE) 2.2 (2013): 21-26