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Designing a Supply Voltage Sensor of High-Resolution for FPGA

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Abstract--- *the integration densities are higher in integrated circuits (ICs). The synchronization of switching activities is done by using a single global clock as one of the main causes that results in the voltage drop across integrated circuit's power distribution network (PDN). Since a circuit's delay is increased by drop, timing failures may occur because of such drops that causes the malfunctioning of IC. Thus, it is essential to use a tool for supporting failure debugging. A supply voltage sensor having high resolution is presented in this paper which has real time failures of debugging and timing margins are determined for critical designs of timing. This voltage sensor is made up of standard "Look-Up Table (LUT) cells" and has dedicated carry cells having propagation delays of high speed. The supply voltage sensor has a voltage resolution of about "3.3 mV on a Xilinx FPGA Spartan-6 (XC6SLX9)".*

Index Terms--- *look-up table, power distribution network, ring oscillator, voltage sensor.*

I. INTRODUCTION

The advancement in modern CMOS technologies over past few decades has led to an increase in the densities of integration circuits (ICs), all because of the nanoscale technology. There has been an increase in the switching currents that is synchronised by a global clock's switching activities[1]. The low requirements of power are fulfilled by scaling down the logic cores inside an integrated circuit. This results in narrowing of timing margins of digital circuit designs of those integrated circuits. This results in the critical correct functionality of ICs. The circuit designers of FPGA were allowed to define voltage values and valid temperatures for generating the timing model. This option is not supported by all the architectures. Instead, a default value is used which is validated within a typical condition of working within 5% range of supply voltage variation for generating parasitic parameters of a circuits such as interconnection delays and cell delays for the best and worst case timing analysis. A default value is used in a working condition that lies within 5% of variation of the supply voltage for generating parasitic parameters. Thus, this variety of variations is degraded by knowing target circuit performance. Thus, reliability of a target circuit increases by putting more number of timing margins for increasing the safety of those circuit operations where digital circuit's reliability is highly affected by EMI and noise [2][3]. The margin which is enough for guaranteeing integrated circuit's correctness is identified by sniffing the voltage variations during operation of circuit in the critical case. Based on both the bounds of voltage variations, the margins for circuits can be established. The variations in supply voltage can be detected by a

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traditional ring oscillator (RO). All thanks to a relationship between cell delay and supply voltage [4]. However, a traditional RO is capable of detecting average variations of voltage during a long time period. A supply sensor of voltage variation has been presented by a gated RO [5]. The resolutions of fine grained delay are obtained by utilizing full custom cells as they are better than FPGA based designs. A "delay line" is used in a supply voltage sensor, also called a "time digital converter (TDC) [6]. A voltage resolution of 29mV can be used for detecting voltage variations cycle-by-cycle. A voltage resolution of 3.9mV exists in sensor's ASIC version [7]. A standard "Look-up Table cells (LUT)" and high speed carry cells are used in a supply voltage sensor. On Xilinx FPGA Spartan-6 kit, the voltage resolution was resulted to be 3.3mV.

II. PRELIMINARIES

II.I. FPGA Structure

A reconfigurable hardware whose functionality is capable of being reprogrammed a number of times is FPGA. It has a better performance than software but lesser than function's implementation in ASIC style. It is typically used as a prototyping platform but also as SoC's core part for energy efficiency and better performance than software and hardware implementations.

IV.I. High-Speed Carry Logic in an FPGA

Being a reprogrammable platform, FPGA is not being of optimized more than the implementation of ASIC style circuit. Such kind of performance issues can be overcome by adopting functional modules and optimized circuit by FPGAs such as block memory, DSP logic and "high-speed carry logic (CARRY4 in a Xilinx FPGA)". By using IP modules of high speed, implementation of high performance circuits on FPGA can be done.

III. PROPOSED METHODOLOGY

The high speed arithmetic logics are supported by a small value of carry propagation delays by using dedicated CARRY4 chains for commercially used high end FPGA families and Xilinx Spartan-6s. A carry propagation wire path has carry generation circuit of 4 bits implemented with it in a CARRY4 cell. A CARRY4 cell has a propagation delay of about 134ps. Delays of short wires are included in this delay and is used for configuration of CARRY4 cells that is used in delay measurement. A propagation delay of about 33.5 ps exists in every carry cell of a CARRY4 cell. There are four carry cells in a CARRY4 connected in cascade. The fine grained delay elements are obtained by taking an advantage of carry propagating logics of high speed can be taken for the construction of delay line or delay chain. However, if a dedicated CARRY4 chain is used then it will lead to the prolongation of delay chain's length and increase of the chip area. Besides, larger delay cells are used for increasing accumulated delay instead of increasing the value of clock period. Large delay cells such as LUTs are used for sensing the variations of voltage. Thus, a delay chain is proposed having two distinct delay granularity. The first part has delay elements that are implemented by using LUT primitives on an FPGA used for the control of coarse-grained delay step and second part comprise of delay elements

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that are based on CARRY4 cells for the control of fine grained delay step. Figure 1 illustrates a delay chain's detailed structure.

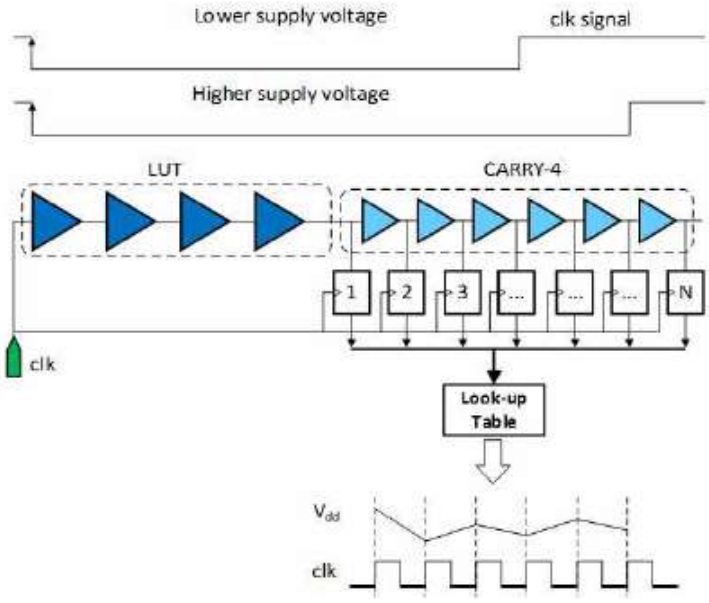

Fig. 1 A supply voltage sensor schematic

There are LUT primitives in first part of a delay chain and CARRY4 cells exists in the second part of a chain. A "phase locked loop (PLL)" helps in the generation of a stable clock signal event in sensor, which propagates over a delay chain and a clock is used for FFs for capturing values of outputs of delay elements. A half of clock cycle fits in the value of sensor's total propagation delay at a minimal supply voltage level. At a rising edge of clock, FFs capture stable values at delay cell. A specific pattern of "000…000111…1" is observed by the values captured at FFs. The operating supply voltage a speed over delay chain that is proportionally affected by it based on the speed of signal propagation. The signal propagation's speed can be detected from the pattern by checking the presence of transition of pattern "0 to 1". Finally, the supply voltage's corresponding speed is derived by looking up at the pre made pattern of mapping table of supply voltage. The table 1 consists of contents of a calibration table.

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Table 1 Calibration Table

Supply Voltage (V)	54-bit Calibration Code	Supply Voltage (V)	54-bit Calibration Code
1.22	0x0000000000001	1.12	0x0000003FFFFFFF
1.21	0x000000000000F	1.11	0x000003FFFFFFF
1.20	0x000000000003F	1.10	0x00000FFFFFFFF
1.19	0x0000000000FF	1.09	0x0000FFFFFFFFF
1.18	0x0000000000FFF	1.08	0x000FFFFFFFFFF
1.17	0x000000000FFFF	1.07	0x003FFFFFFFFFF
1.16	0x000000003FFFF	1.06	0x01FFFFFFFFFFF
1.15	0x00000000FFFFF	1.05	0x07FFFFFFFFFFF
1.14	0x0000000FFFFFF	1.04	0x1FFFFFFFFFFFF
1.13	0x0000003FFFFFF	-	-

IV. EVALUATION OF PERFROMANCE

- Validity of a supply voltage sensor

The operation is validated and voltage resolution is evaluated for a supply voltage sensor by changing the FPGA logic core's (VCCINT) operating supply voltage intentionally. The internal core's VCCINT pin is connected to programmable supply of DC power and voltage is changed with a step of 10mV from a value of 1.04V to 1.22V. The experimental setup of measurements is shown in figure 2.

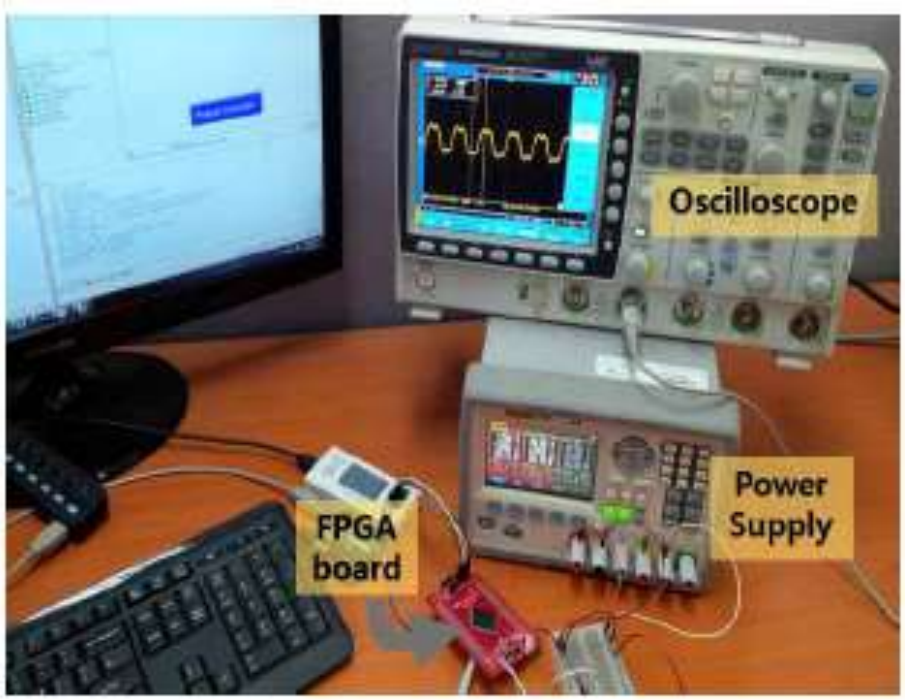

Fig. 2 Setup for experimental measurements

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There is an increase and decrease in the 0 bits stored in delay chain's FFs when supply voltage is decreased or increased. The clock has its falling edge faster over a chain with the decrease in the delay chain's propagation delay with an increase in supply voltage. There are large number of 0 bits that are capable of passing through a delay channel. If the supply voltage is decreased then it leads to an increase of propagation delay. It leads to the slow propagation of clock signal's falling edge and thus, a decrease of 0 bits that pass through a delay chain. The result of measurements are given in figure 3. The green circle represents actual results of the measurements. There is a linear relationship between operating supply voltage and 0 bits that pass through a delay chain. A fitted curve is obtained by using data of measurement and a red line having slope of 0.0033V represents the measured data.

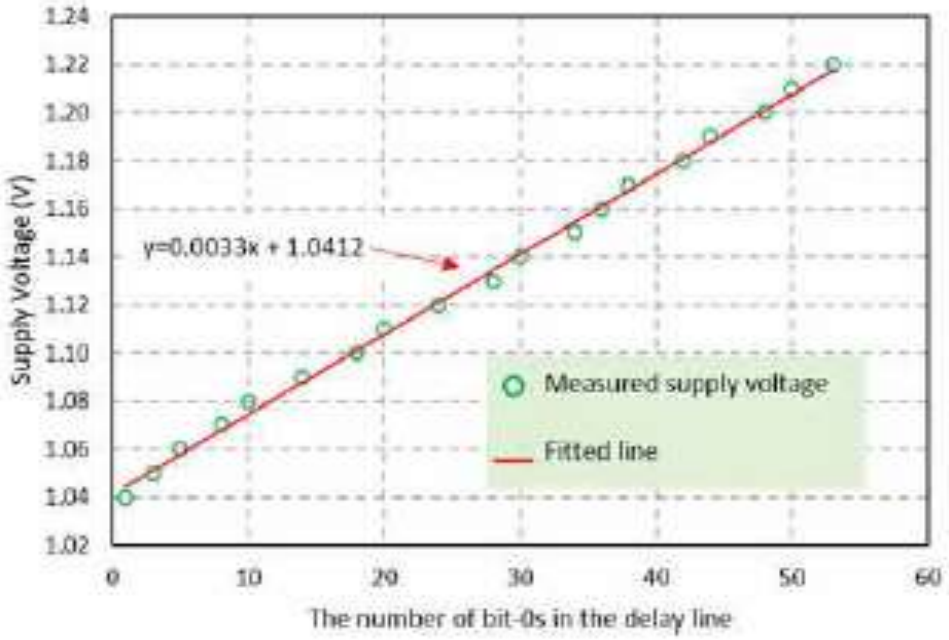

Fig. 3 Measurement of supply voltage

Table 2 Comparison between resolutions of voltage

Refs	FPGA/ASIC	Tech.	Resolution (mV)
[6]	Altera Stratix III	65nm	29
[7]	ASIC	65nm	3.9
[9]	ASIC	45nm	7.6
[10]	ASIC	90nm	10.0
[11]	ASIC	90nm	20.0
Ours	Xilinx Spartan-6	45nm	3.3

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The comparison between voltage resolution of this and previous work is given in table 2. It is clearly seen that the voltage resolution of this work is much better than previous works [6][7][8][9][10].

V. RESULT

The figure 4 shows a block diagram of target design. The power hungry circuits that are capable of consuming big quantity of dynamic supply currents simultaneously. Therefore, voltage drops occur across a target circuit's PDN and the original operating voltage across target circuit's PDN drops and the values. Large quantity of dynamic supply currents are consumed by power hungry circuits of dummy logics. Therefore, voltage drops occur across a target circuit's PDN. The dummy logic blocks are activated or deactivated individually in an independent manner and target design is controlled for writing into memory the measured results. The stored results are transferred to an external memory by an on chip UART transmitter. Figure 5 shows the measurement results. At the execution's initial part, no drop in voltage drop is observed because neither logic block is activated. The second part is marked by DL-1 and when it starts the operation, it results in the voltage drop. This part results in the voltage drop of about 20-30mV. The voltage drop is observed around 20-30mV. Similarly, there is a drop in supply voltage of about 50 to 70-80mV leading to the activation of logic blocks in turn.

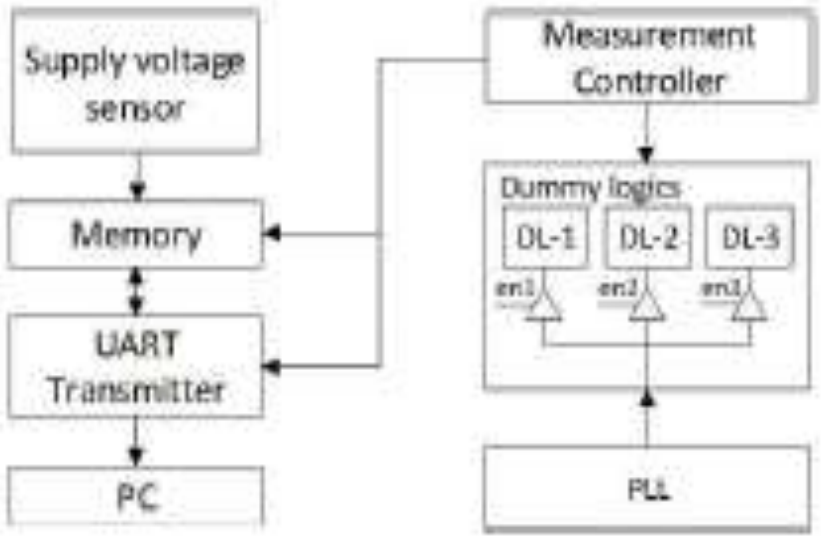

Fig. 4 Supply voltage drop evaluation

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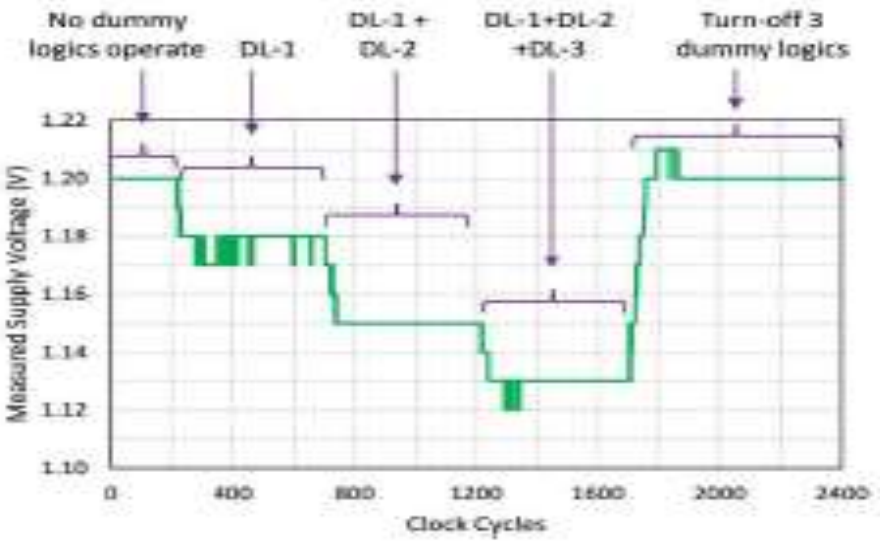

Fig. 5 Results of voltage drop measurement

The size of circuit of dummy logic blocks is same as that having 1000 FFs in every block. The only difference that exists in between them is of clock routing and data. Thus, a slight difference of current consumption from each other exists. The dummy logics operate at a frequency of 60 MHz.

VI. CONCLSUION

A high resolution supply voltage sensor which is synthesizable on FPGA is presented in this paper. Its functionality is verified and a profile of voltage drop is detected for target design. The circuit has been implemented on Xilinx Spartan-6 (XC6SLX9). The voltage resolution is obtained to be 3.3mV because of "fine grain delay resolution". The voltage sensor designed in this work has a better resolution of sensing when comparison is done with previous work [6][11] and [12]–[15]. The highly reliable digital circuits employ proposed methodology for safety critical system that work in noisy and harsh environment such as car's airbag control system and airplane's cruise control system.

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