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Classifying 6T SRAM Cell over Processing Voltage and Temperature Curves

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Abstract--- *According to the shifting of centre of mass of the semiconductor firm headed for multimedia, consumer and communications applications, different requirements in term of memory have ascended. The incomparable need for memory being mostly compelled by computer industry. Power consumption is pretty limiting factor for quantity of memory that can be integrated on the single board. This project scrutinizes and classified six transistor SRAM cell over processing temperature and voltage dissimilarities. The parameters of a SRAM being considered are as Read Delay, SNM Read, Write Delay, leakage power dissipation and SNM Write.*

Index Terms— Read Delay, SNM Read, Write Delay, leakage power dissipation, 6T SRAM cell and SNM Write.

I. INTRODUCTION

Multiple VLSI chips[1] having vital components of Static Random Access Memories (SRAM)[2]. Storage had been broadly consumed in almost every electrical and electronics systems/devices which is: microcomputers, mainframes and mobile phones etc. with technological procedure developing in submicron region that supports Moore's Law, storage capacity on single chip is developing day by day. Microcontrollers and microprocessors proves the increment in generation of bridge the increasing gap into the speeds by processor & key memory[3].

Furthermore, power consumption had become very important consideration both with increasing level of integration and operating speeds and also due to the remarkable development of battery functioned devices. The particular project focuses in classification of 6T SRAM cell in 0.19 µm into CMOS technique[4].

Wherever procedure & supply clambering remains greatest drivers by low energy structures, this project researches a few systems which is being utilized related to scaling to accomplish low power application[5].

Principle goal of this project for planning 6T SRAM cell & to enhance for read and compose execution. The subsequent goal is to portray this SRAM cell crosswise over procedure, voltage and temperature corners.

II. LITERATURE REVIEW

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II.I 6T SRAM Cell

Superior SRAM's are very pivotal part in the memory pecking order of current figuring frameworks. This structure centres around three constraints process voltage & temperature varieties in 0.18µm CMOS innovation[6].

For procedure varieties "TSMC 180nm CMOS" procedure has been contemplated. Procedure varieties that results into accompanying blends which is: "typical nmos - typical pmos , slow nmos – slow pmos, fast nmos – fast pmos , slow nmos – fast pmos and fast nmos – slow pmos".

Additional concern is temperature, i.e., ordinarily gadgets are capable of playing out their best at - 4°C to 60°C. Consequently, face issue on cold places where temperature is less at that point - 4°C. The recommended task will work on - 20°C to 80°C temperature.

An additional constraint stands voltage. The planned SRAM cell works by way of supply voltage of 1.8V ±10%[7].

The suggested project creates straightforward numerical models by "process, voltage and temperature" by 6T SRAM cell & check these alongside SPICE circuit re-enactments. The innovation under thought for this examination is a 0.19 µm CMOS TSMC process[8].

II.II Working of 6T SRAM Cell

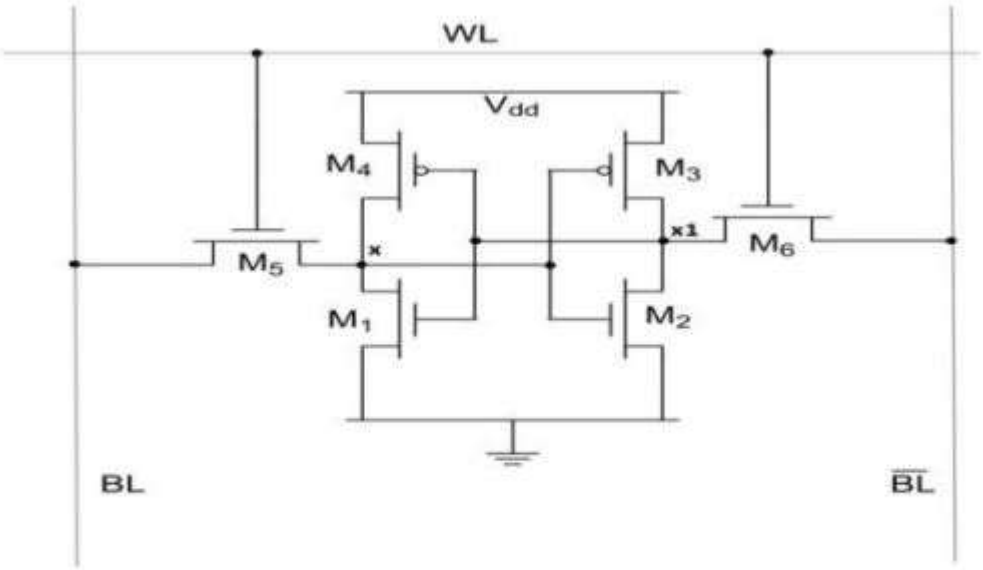

Fig. 1: 6T SRAM Cell

A control-level circuit to customary "6T SRAM storage cell" is appeared. Overhead memory cell frames the reason for most static arbitrary access recollections. 6 transistors are employed for storing and accessing single bit information.

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Four transistors inside structure 2 cross-interlinked inverters. In genuine gadgets, these transistors prepared in least component sizes for reducing area of circuit. Because of cross-coupled construction, a “low input voltage” esteem on the main inverter will creates high voltage esteem on the subsequent inverter, which increments and recoveries the low voltage esteem on the subsequent inverter. In like manner, a high info voltage esteem on the primary inverter will create a low information voltage esteem on the subsequent inverter, which is criticism as the low info esteem onto the principal inverter. Accordingly, two cross-coupled inverters that spares & hold their current intelligent worth. “Word line and bitline” are associated through access transistors to peruse and keep in touch with cross-coupled inverter[9].

II.III Read Operation

Whenever word line at logically high value, both of the n-transistors are turned ON and are attached with input and output of the inverter to two bitlines. This implies that, both inverters powers the present information “logical value stored” in “SRAM cell” on said bit line & the transformed information consistent incentive on the “inverted bit line”. This information worth is then expanded along these lines producing the yield intelligent estimation of said “6T memory cell” into read task[10].

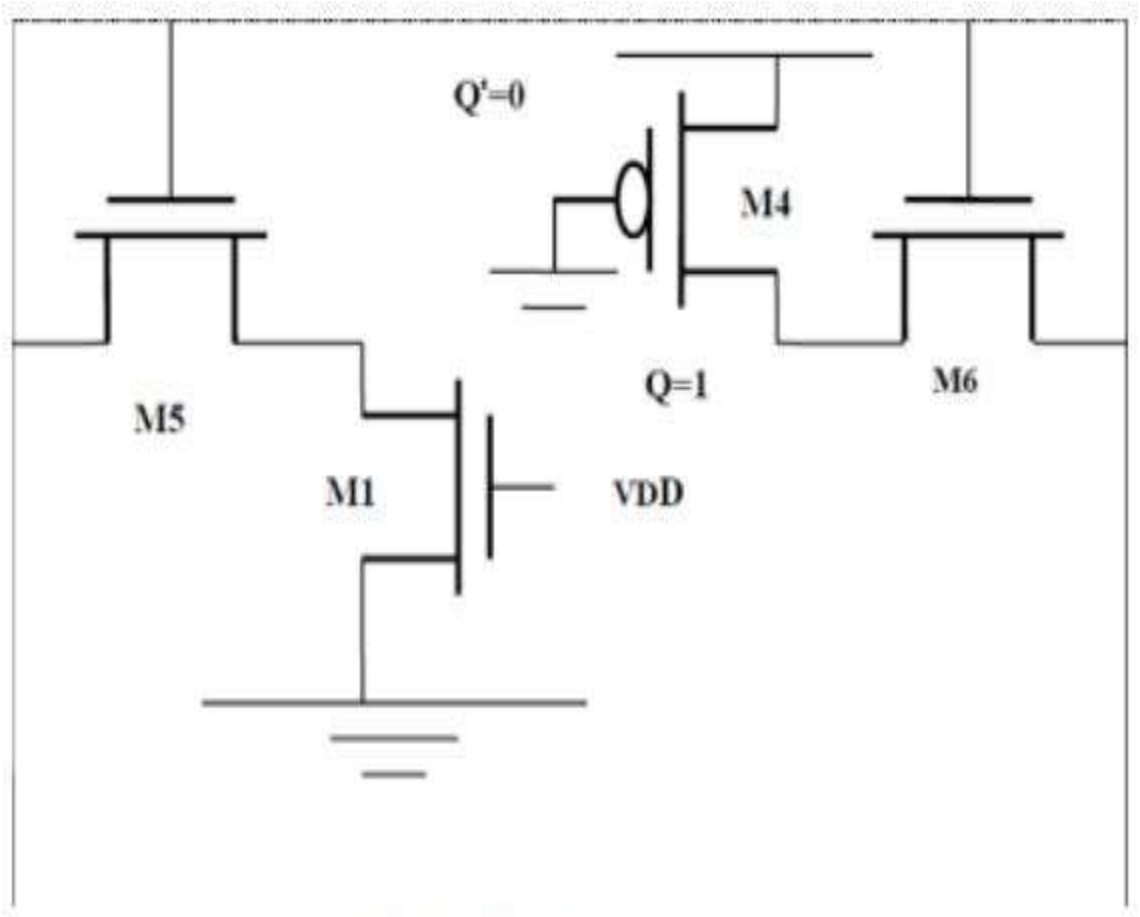

Fig. 2: Read Operation

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II.IVWrite Operation

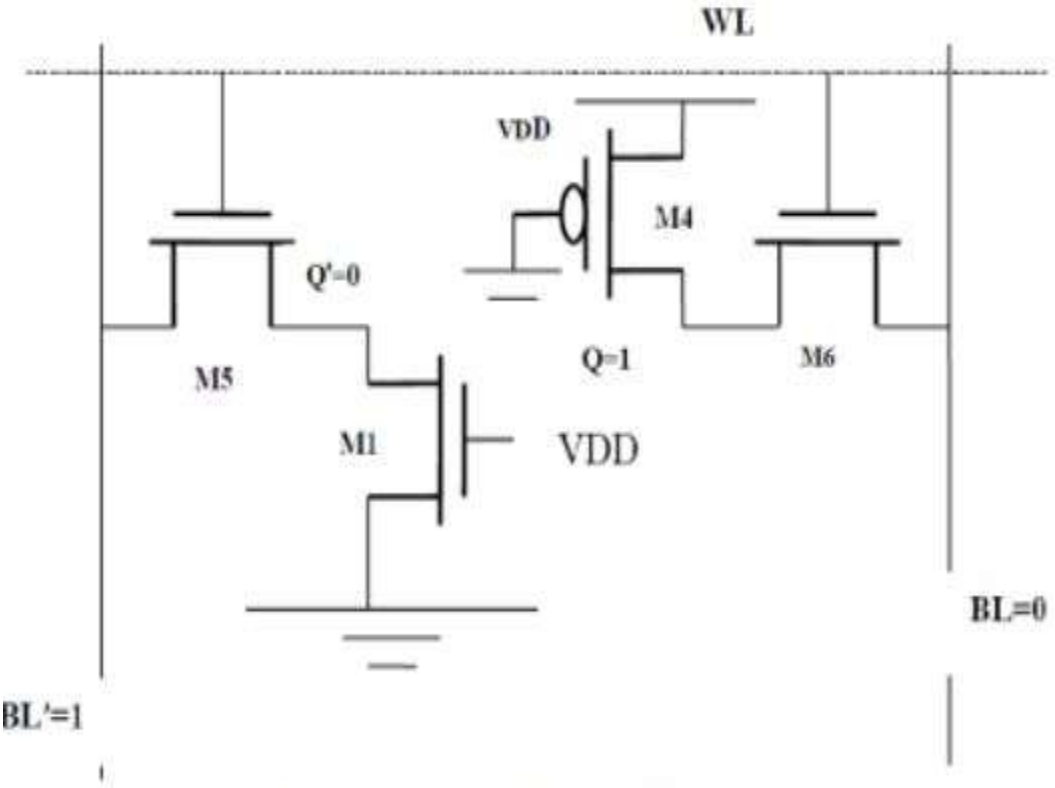

Fig. 3: Write Operation

For inscription of renewed data in the "storage cell", a logically high value is provided to word line, and activation of bit line drivers are also performed. On the basis of stored logical value there may be a short circuit in the SRAM cell, and thus the stored "logical value" gets overwritten.

III. 6T SRAM CELLLS CONSTRUCTION

For the calculation of W/L parameters in MOS transistors of CMOS SRAM cell construction principles should be considered.

A) Data reading action must not be abolish stored data into the SRAM cell.

B) The stored data modification must be allowed during the data write phase.

For the small geometry techniques while "read access" & "standby mode" for preserving the data of the memory cell being essential well-designed production. The smaller supply current makes the memory cell unstable which results increment in leakage currents & incrementing temp. Changeability, that results from technological scaling. The stability of signal to noise margin is highest rate by the DC noise voltage which is abided by SRAM cell deprived of fluctuating stockpiled data bit[11].

The capability of overwriting data in the storage cell the inscribe margin is demarcated by means of measure.

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Inscribe margin current being an extreme noise current rate available in the bit lines while an accurate inscribe action. A failure in inscribing happens whenever the inscribe margin voltage exceeded by the noise current. In this segment, the static approach is being approached for calculating inscribing margin[12].

III.I Simulation Results

Previous SRAM cell had been verified by employing simulating in SPICE in 0.19 µm regular CMOS TSMC development technique.

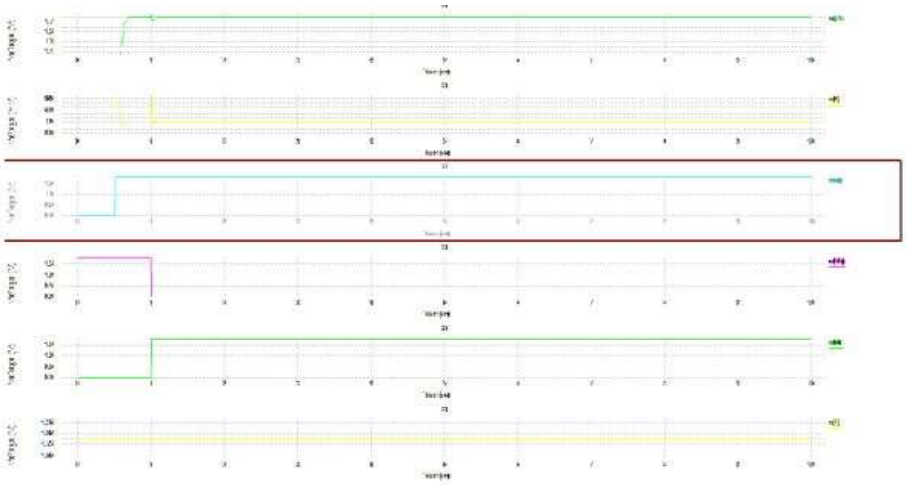

Fig. 4 : Read Results

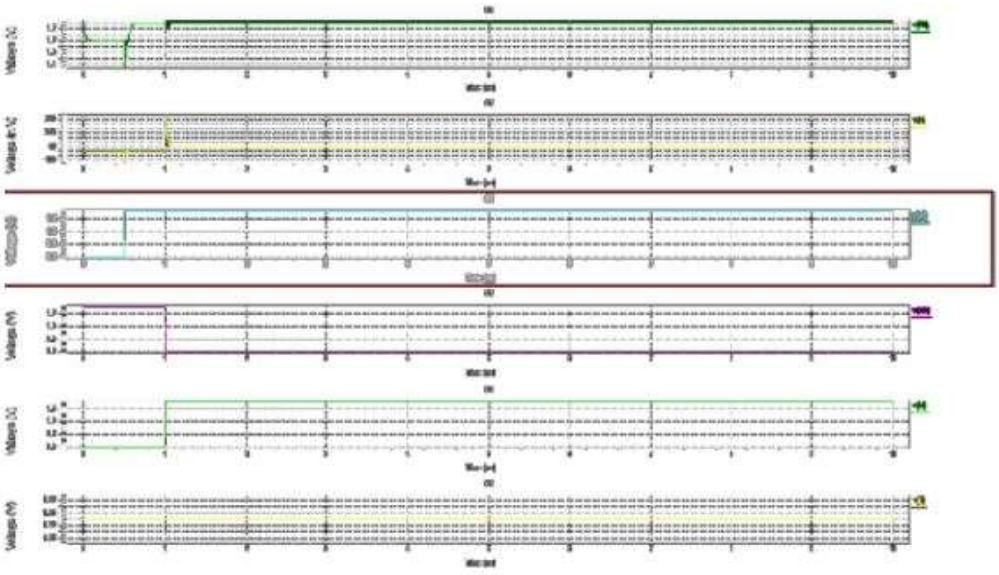

Fig. 5: Write Results

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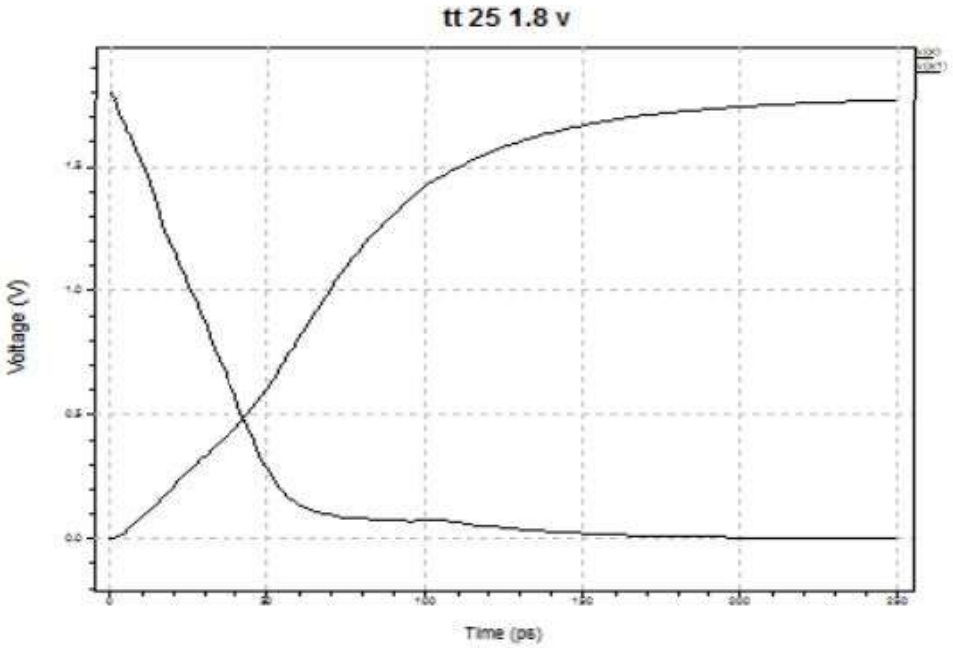

Fig. 6: Butterfly curve for TT, 25 °C, 1.8V

III.II Characterisation Graphs

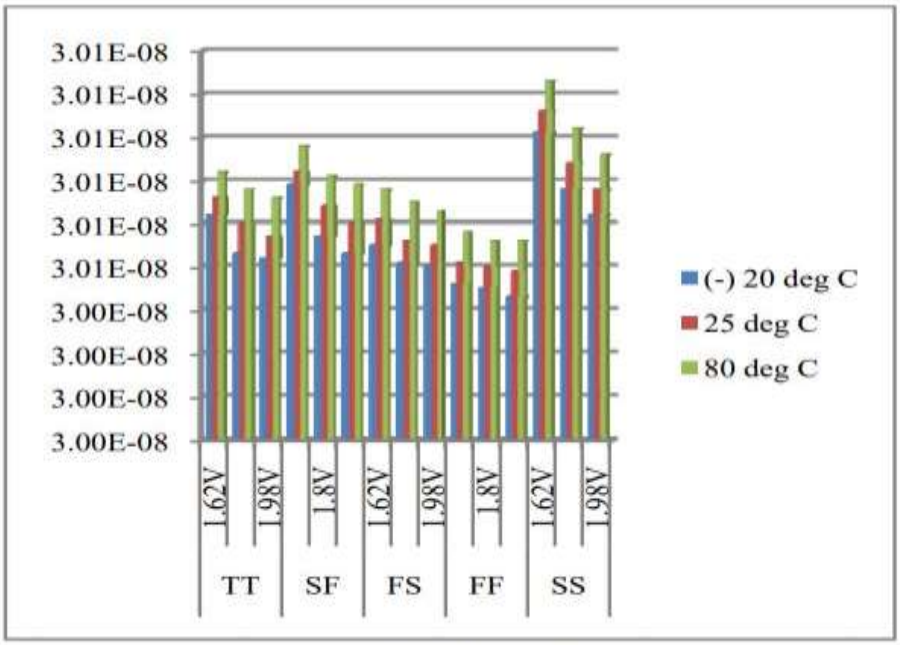

Fig. 7: Read Delay in sec

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These are "characterization graphs" of variable SRAM constraints through procedure dissimilarities "(viz. Typical nMOS-Typical pMOS TT, Slow nMOS-Fast pMOS SF, Fast nMOS-Slow pMOS FS, Fast nMOS-Fast pMOS FF and Slow nMOS-Slow pMOS SS); temp. Dissimilarities (viz. -20 º C, 25 º C and 80 º C)" and verities in power supply of ± 10%.

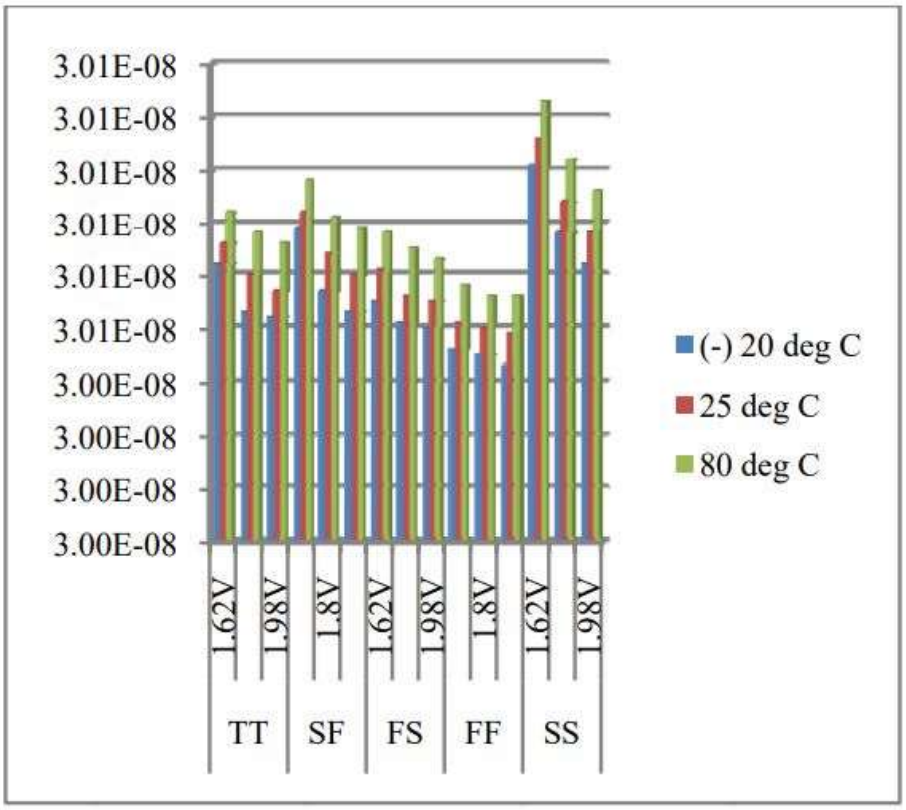

Fig. 8: Write Delay in sec

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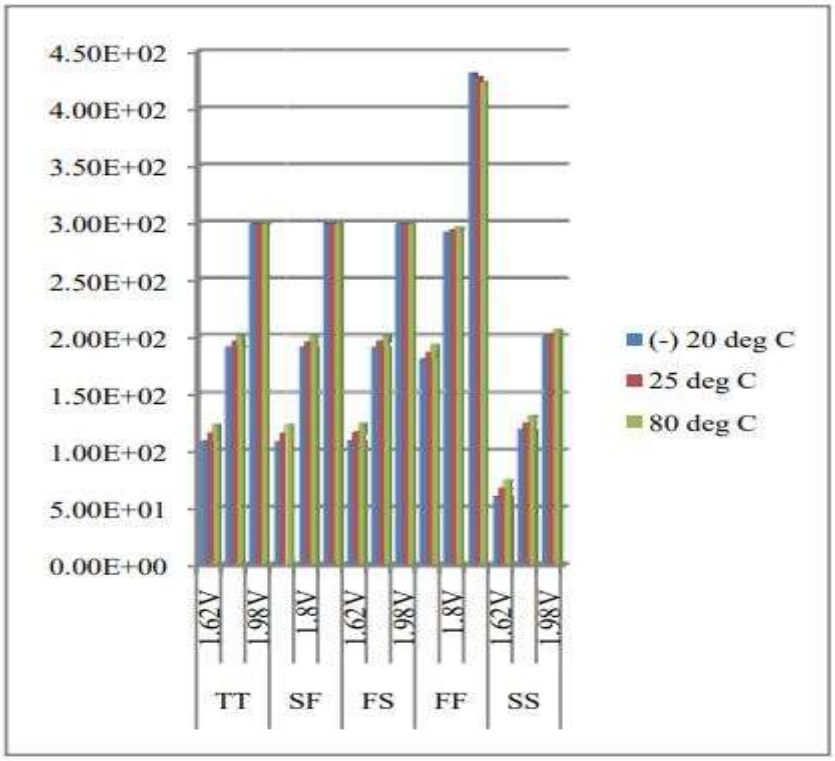

Fig. 9: Leakage Power in µWatts

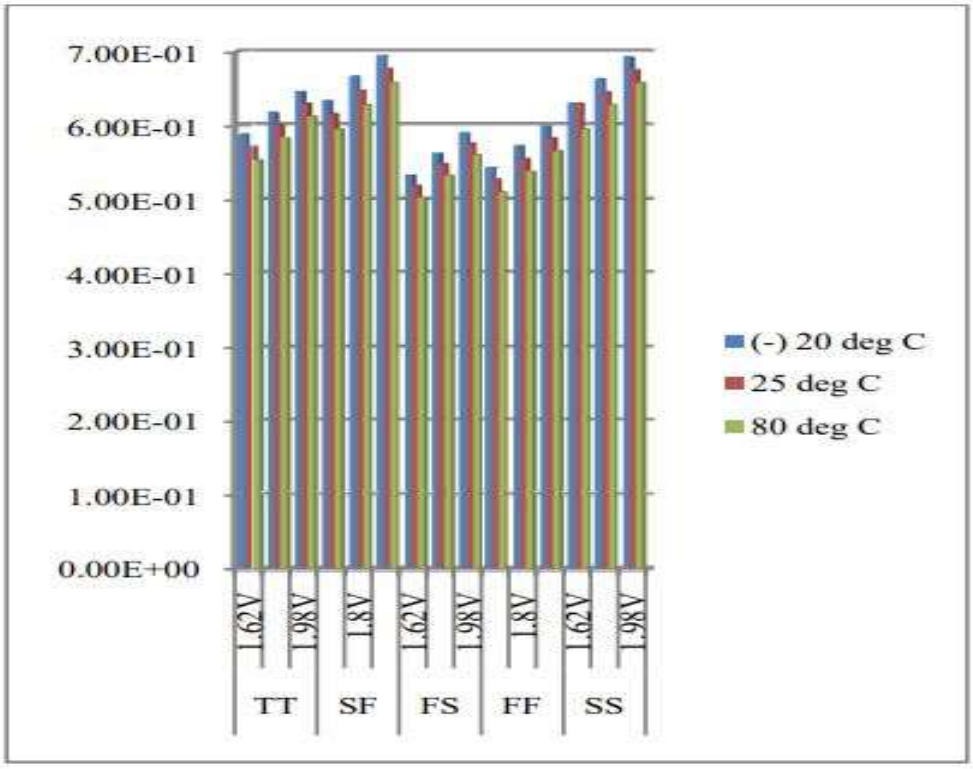

Fig. 10: SNM Read in Volts

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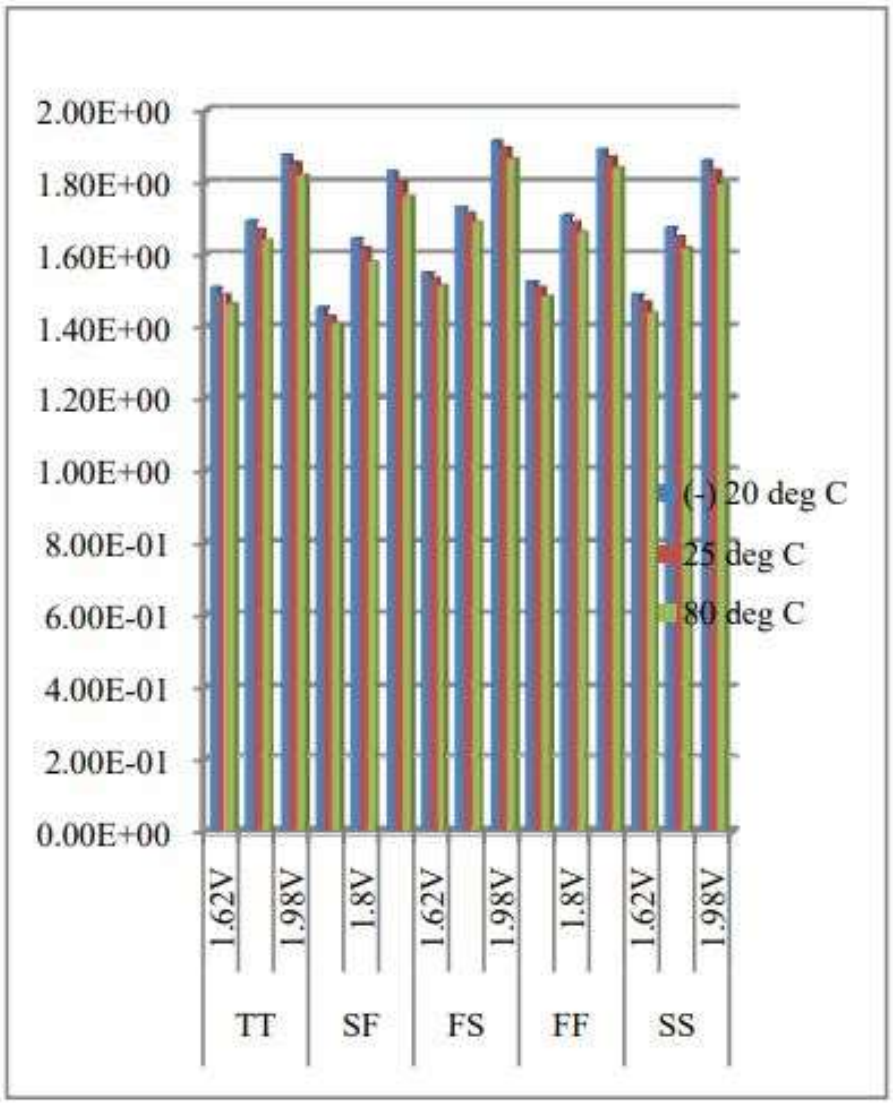

Fig. 11 : SNM Write in Volts

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III.III Resulting Table

Table 1: Characterization Table

Parameter	Best Case Scenario		Worst Case Scenario	
	O/P Value	Process, Voltage ,Temp	O/P Value	Process, Voltage, Temp
READ Delay (sec)	3E-8	FF,1.98V,-20ºC	3.01E-8	SS, 1.62V,80º C
WRITE Delay (sec)	3E-8	FF,1.98V,-20ºC	3.01E-8	SS, 1.62V,80º C
POWER DISSIPATI —ON	-59.32u	SS,1.62V,-20ºC	-430.87u	FF,.98V,-20ºC
SNM READ (V)	0.658V	SF ,1.98V,80ºC	0.502V	FS,1.62V, 80ºC
SNM WRITE (V)	1.91V	FS,1.98V,-20ºC	1.41V	SF,1.62V, 80ºC

IV. CONCLUSION

The proposed project performs classification and analyzation by present "6T SRAM cell" for reading and writing operation for the speed and highly profitable performance, on chip "caches memories" in 0.19 µm "CMOS TSMC process". Figure 6. Shows the voltage and time curve, this curve indicates that the voltage increases with increase in time and at a point (1.5 V) the voltage almost attains its maximum value ate 200 ns.

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