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An experimental approach of Power Proficient, High Gain R-2R Ladder DAC and Designed in 90nm CMOS Technology

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Abstract--- *In present era of communication system there is a long-felt need for broad band transmission of data (i.e. image, audio or video) at a high rate of data transmission. In this paper an 8 bit D/A converter (DAC) is constructed, simulated in Matlab and compared with the other available DACs. The constructed DAC has very low power consumption of around 2.12 mWatt along with the DNL of 0.40 and INL of 0.78.*

Index Terms*— DAC, DNL, SNR, SFDR, R-2R ladder, Op-Amp, CMOS, INL, DNL.*

I INTRODUCTION

In this high-tech era, the industries based on electronic are growing continuously and utmost maximum signals are analog in nature[1]. All of the characteristics such as speed, time, accuracy, weight etc. are calculated in the analog domain, therefore there is a long-felt need for data converter[2]. In digital signal processing (DSP) the data converter plays a most important role, it joins the analog to the digital world. The digital bit to the analog signal is converted by the electronic circuits, and this circuit is known as digital to analog converter (DAC)[3], and the conversion of analog signal to digital signal is performed by analog to digital converter (ADC). These are the essential converters in terms of DSP, they help the system to improvise the system features such as linearity, accuracy, speed, reliability, area and power.

The SiGe and GaAs are the technologies employed for the construction of high speed data converters. These technologies are not fabricated on single chip and they have manufacturing related drawbacks such as process, power consumption etc. these drawbacks can be overcome by employing CMOS technology[4] with the low supply voltage. Henceforth, the system-on-a-chip (SOC) is prepared on the basis of DSP circuitry with high speed DACs integration in order to reduce the cost of manufacturing.

The DACs dynamic features, for example, signal to noise ratio (SNR), spurious free dynamic range (SFDR) including bending and their static attributes, for example, differential non linearity (DNL) [5]and integral non linearity (INL) are significant in DSP frameworks. In this paper segment II depicts the basic design and structure pf DAC, segment III speaks to re-enactment aftereffects of the simulation result lastly end is written in segment IV.

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II DAC's ARCHITECTURE

Numerous architecture of the high speed DACs are offered in the present-day such as binary weighted, current mode, voltage mode, R-2R ladder type etc. the following requirement such as accuracy, high speed, bandwidth and power consumption must be considered for the high architecture[6]. The construction of the high resolution DAC of the high bandwidth are very complex and have different type of errors namely gain error, absolute error and missing code etc., in such kind of scenario the best performance is provided by 8 bit converter. Simple construction of the DAC is shown in the below stated figure.

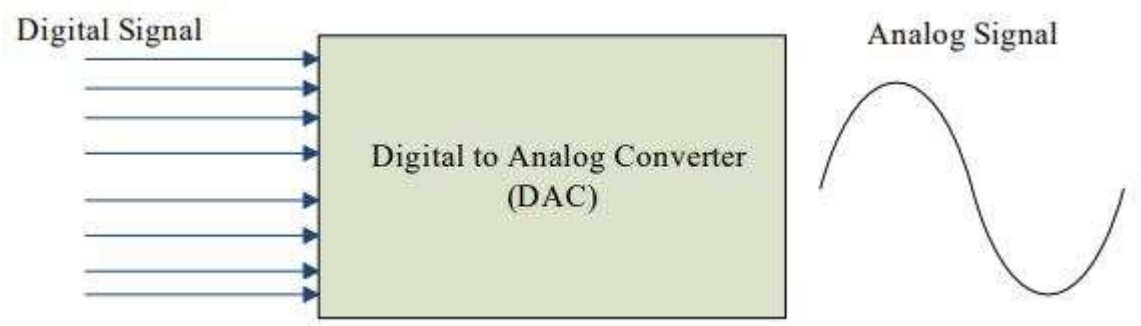

Figure 1: Digital to Analog converter block diagram.

II.I. R-2R ladder DAC (without Op-amp)

The sample of a voltage mode R-2R ladder type DAC converter is shown in the Figure[7].

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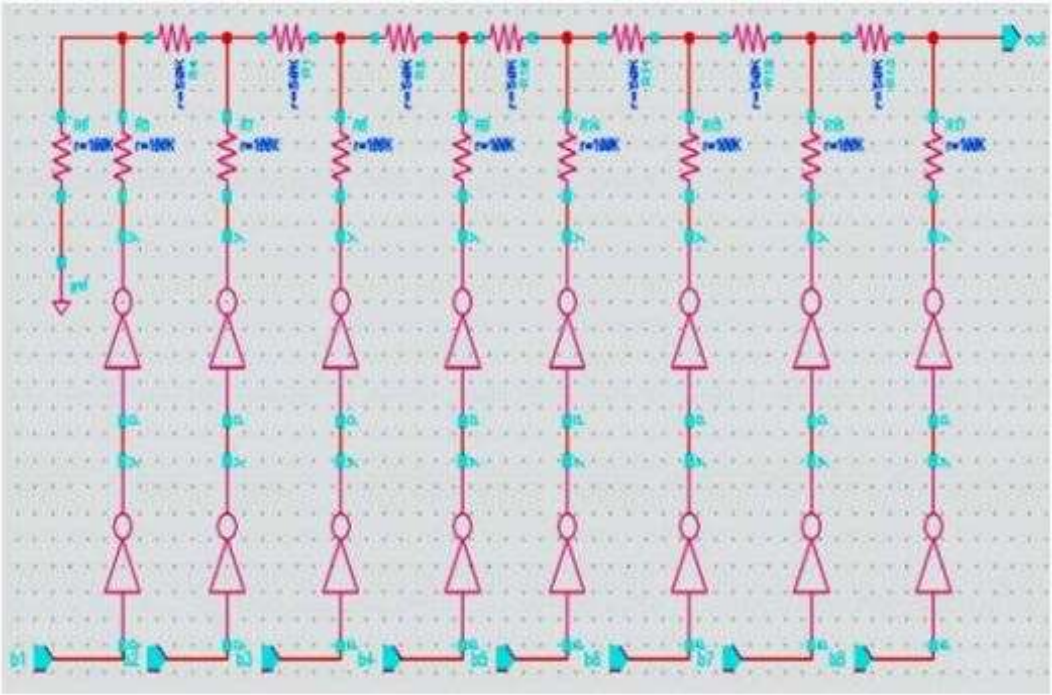

Figure 2: Circuit diagram of the R-2R ladder type DAC

In the particular DAC the output input is constant throughout but the input impedance varies, the output impedance is almost equal to the 'R' of '2R' ladder.

II.II. R-2R ladder DAC based on Op-amp

In the particular DAC, constructed on the basis of the Op-Amp based ladder summing amplifier that is shown in the figure below.

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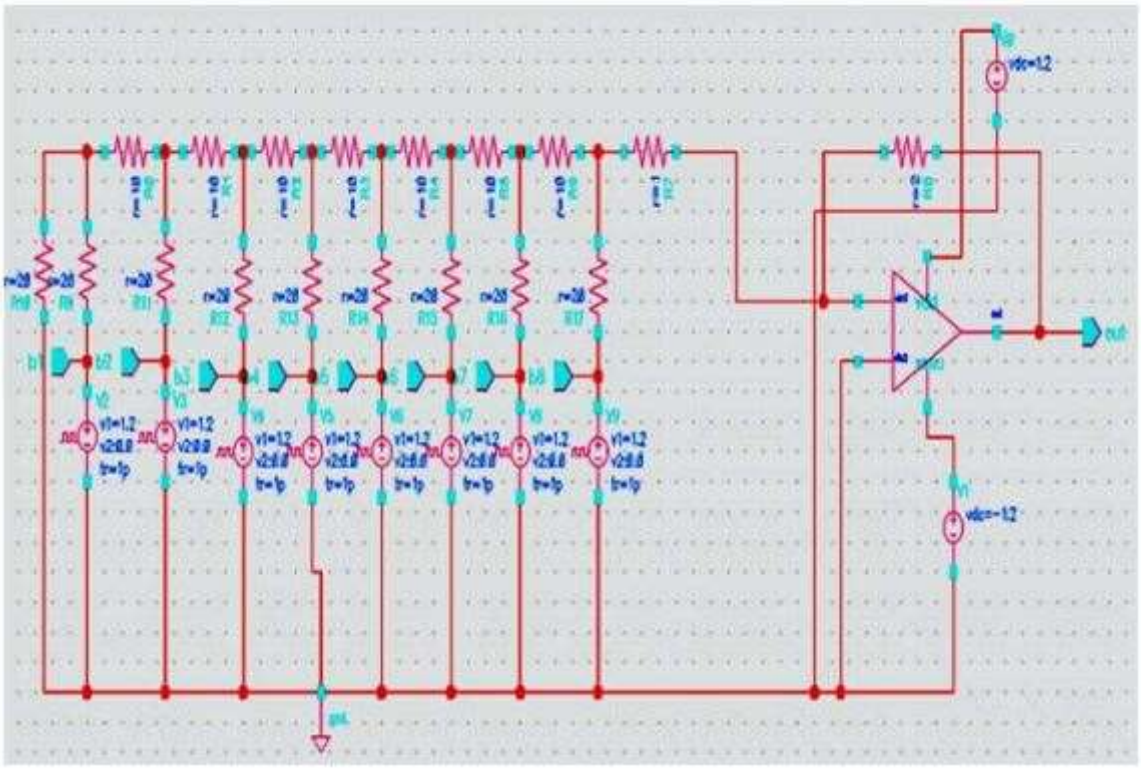

Figure 3: Circuit diagram of the Op-Amp based DAC

III DESIGNING OF OP-AMP

The op-amp is constructed on the 90nm CMOS technology for the implementation of DAC. The op-amp is constructed with the low power consumption and low power supply voltage, as shown in the figure below.

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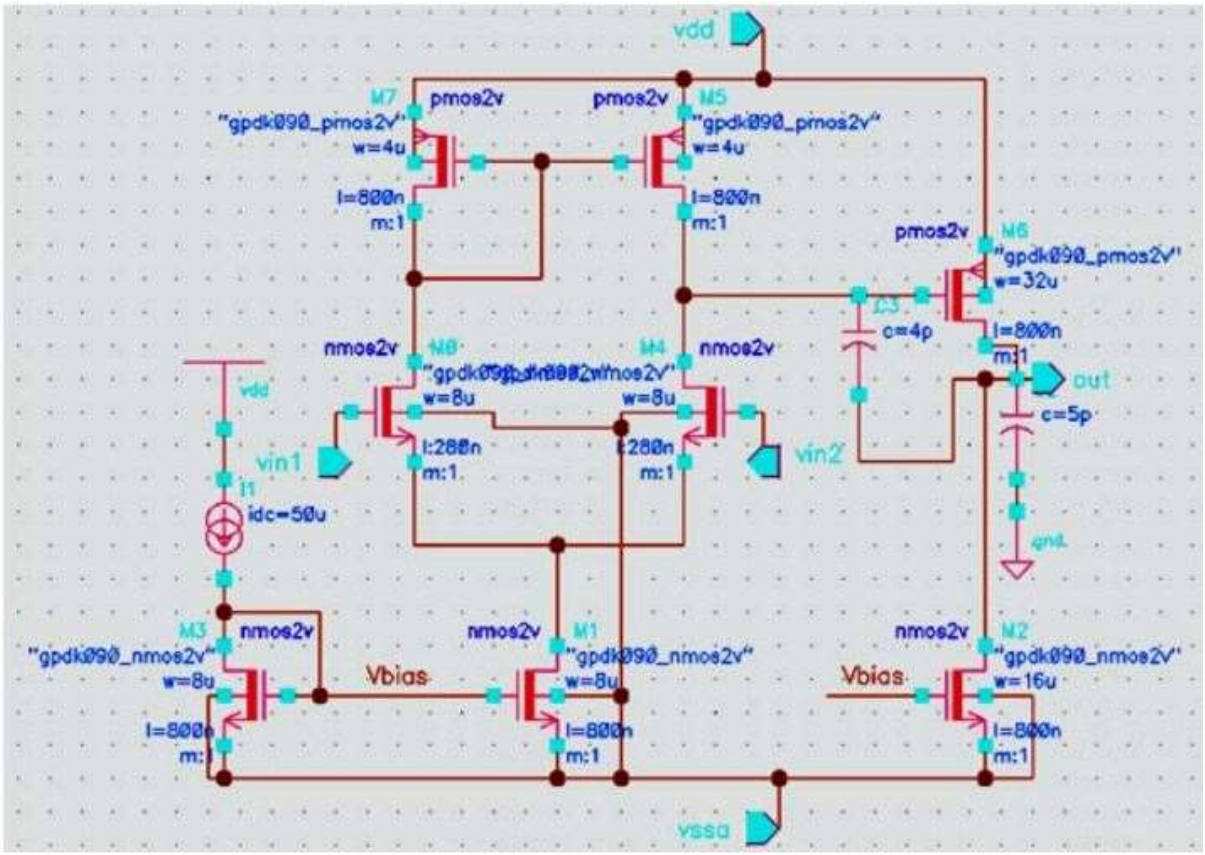

Figure 4: Circuit diagram of the proposed Op-amp for DAC

The most significant building in the analog circuit design. This comprising of the two stages, first one is differential amplifier and the second one is the common source amplifier stated in the figure above. But the supplementary stage add the pole in the right side of the jw axis which creates system unstable. There are numerous of techniques that aid to make system stable, these techniques are Dominant pole compensation technique, Miller compensation technique and enhance phase compensation technique. In this work the Miller compensation technique is employed to increase the gain margin and phase margin. In the above shown figure, the CMRR, low offset, PSRR, high gain with noise and high input impedance is provided by first stage. The adding gain, level shifting and it also behaves as a differential for single ended converter by the usage of second stage. For certain specification the two stage design of Op-amp is provided below:

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Step 1: Choose the value of load capacitor C_l and it must lie between 1pF to 4pF and slew rate find from bias current flow in M1.

$$C_c >= 0.22C_l$$

Step 2: Determine the value of current flow in M1 transistor.

$$SR = I/C_c$$

$$I = C_c \times SR$$

Step 3: Design the transistor M0 and M4 using current equations.

$$(W/L)_{1,2} = g_{m0}^2/u_n c_{ox} 2I_{D1}$$

Step 4: Design the transistor M5 and M7 choosing value of input common mode range.

$$(W/L)_{5,7} = \frac{2I_{D3}}{u_p c_{ox}\left[V_{DD} - (ICMR+) - V_{t\max} + V_{t\min}\right]^2}$$

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Step 5: Design transistor M1 from calculated value of V_{Dsat}

$$V_{Dsat} >= ICMR(-) - (2I_{D1}/ß_1) - V_{tmax}$$

Using the calculated value of V_{Dsat} design the M1,

$$(W/L)_1 = \frac{2I}{u_n c_{ox} (V_{Dsat})^2}$$

Step 6: Design transistor M6 by calculating gm6 and gm5.

$$g_{m6} \geq 10 g_{m0}$$

$$g_{m5} = \sqrt{u_p c_{ox}} (W/L) 2I$$

$$(W/L)_6 = \frac{g_{m6}}{g_{m5}} (W/L)_5$$

Step 7: Design transistor M2, first calculate the I_6,

$$I_6 = I_2$$

$$\frac{I_6}{I_5} = \frac{(W/L)_6}{(W/L)_5}$$

$$\frac{I_2}{I_1} = \frac{(W/L)_2}{(W/L)_1}$$

$$\text{First stage gain} = \frac{g_{m5}}{g_{ds4} + g_{ds5}}$$

$$\text{Second stage gain} = \frac{g_{m6}}{g_{ds2} + g_{ds6}}$$

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Construction specification defined which are most important to get preferred response of op-amp, shown below in table 1. The minimum power dissipation with maximum gain and good phase margin can be obtained by changing some required features such as sizing or transistor, size also matters as every transistor width increases its size which build the transistor very heavy and acquires more space, the sizing of transistor feature as shown below in table 2.

Table 1: Specifications for designing of two stage op-amp

S.No.	Parameters	Value
1.	V_{DD}	1.2
2.	ICMR(+)	0.8
3.	ICMR(-)	0.5
4.	Gain bandwidth product	20MHz
5.	Open loop gain	60db
6.	Phase margin	60
7.	Slew rate	20v/us
8.	Load capacitance	5pf

Table 2: Effect on gain and power dissipation by varying feature size

I_{DC}	$W_{0,4}$	$W_{5,7}$	$W_{1,3}$	W_6	W_2	Gain(db)	Power dissipation
30u	15u	20u	10u	20u	15u	23.63	62.18u
30u	15u	20u	10u	25u	13u	31.4	67.67u
30u	15u	30u	25u	25u	13u	45.93	56.52u
30u	15u	25u	25u	25u	25u	46.03	58.47u

IV SIMULATION RESULTS

The output waveforms of the simulation for DAC based Op-amp and two stage Op-amp as shown in figure below.

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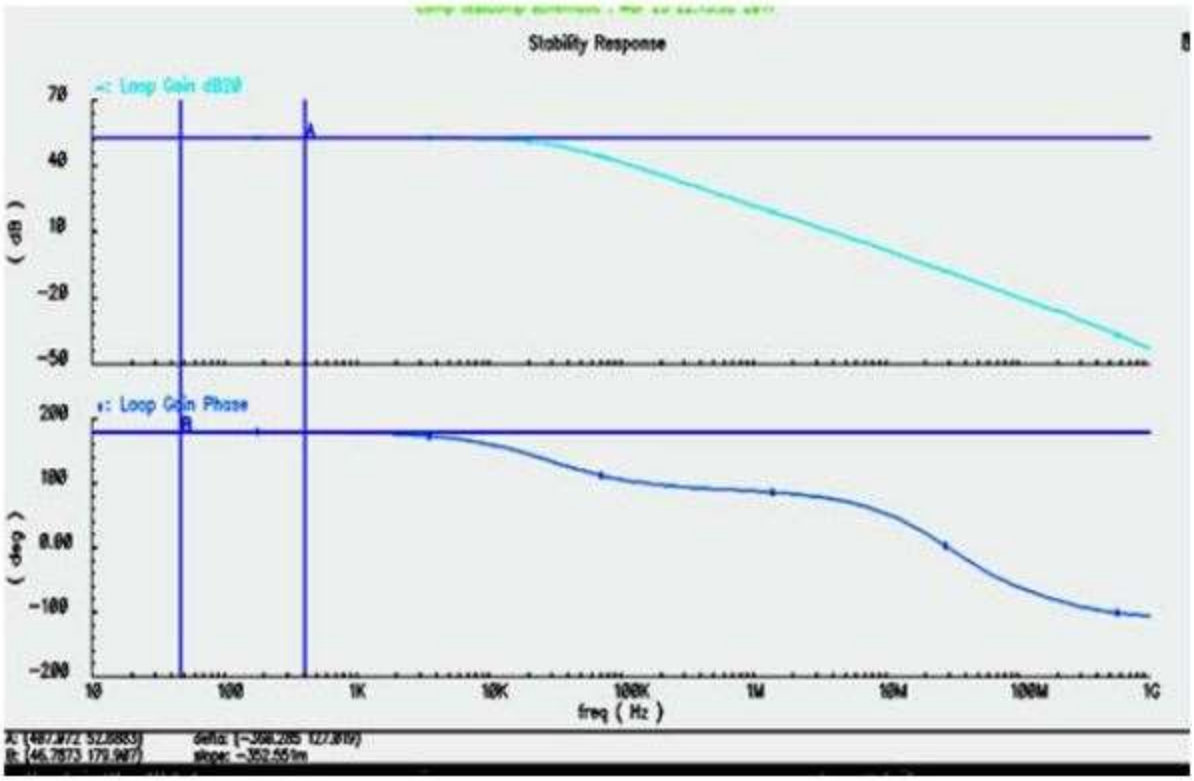

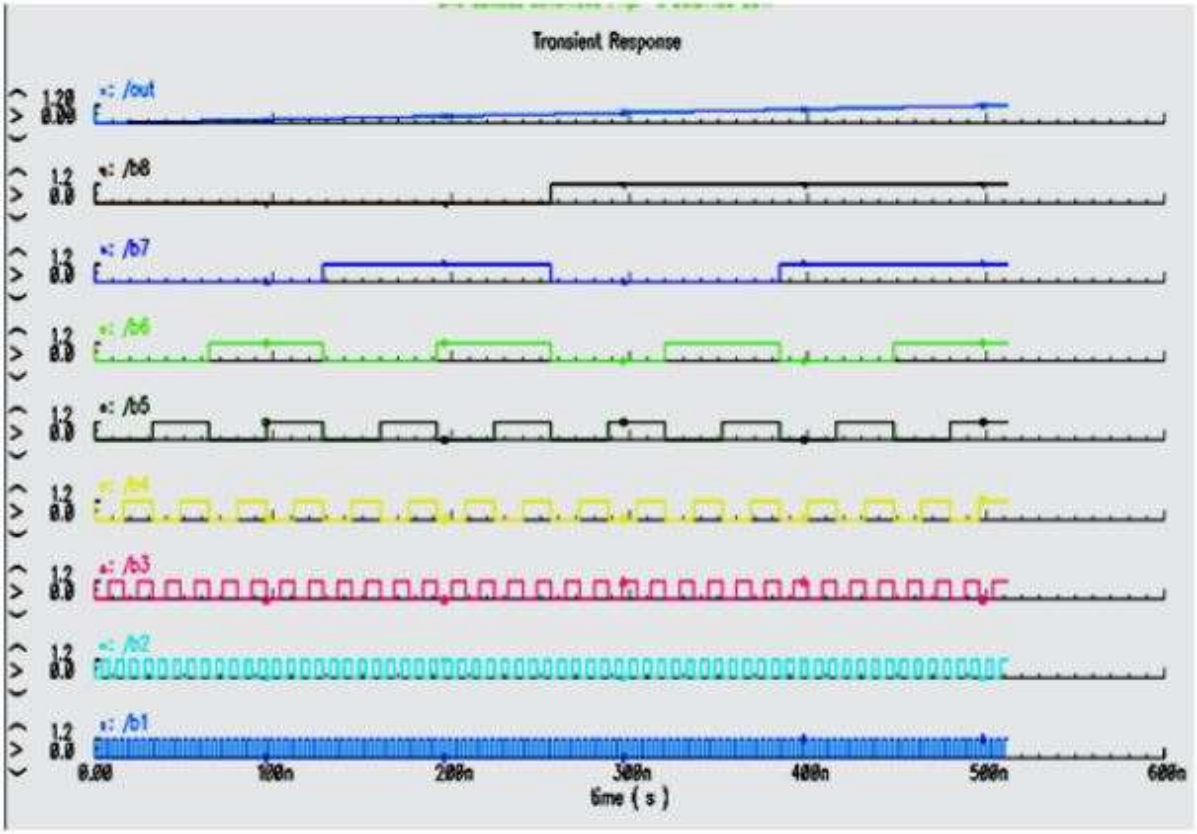

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Table 3: Comparative study on DAC Power dissipation among different research paper.

Specification (Unit)	[2]	[3]	[4]	This Work
Supply Voltage (Volt)	1.2	1.2	1	1.2
Resolution (Bit)	10	12	10	8
Process (nm)	90	90	90	90
Power Consumption (mW)	23	128	49	21.2
DNL	-	0.5	-	0.40
INL	-	1.2	-	0.78

V CONCLUSION

The 8 bit R-2R ladder DAC employing Op-Amp is constructed and simulated in the 90 nm CMOS technology. The Op-Amp is an active device, thus the DAC can be deployed to convert low digital signal to high amplified Analog signals. Beside this, as the construction is prepared in 90 nm CMOS technology, it provides the sufficient power consumption and full output swipe. INL and DNL performance of the constructed DAC is as good as compared to the previously constructed DACs.

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