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Low Power and Low Latency Memristive-Ternary Content Addressable Memory Design Using Absolute Path Search Optimization (APSO) Algorithm

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Abstract--- *In this work, a Low Latency and low power use of memristive ternary content addressable memory (MTCAM) design is implemented for utilizing new optimization method specifically Absolute Path Search Optimization (APSO) algorithm. The outline of a proposed memory has been altered by the expansion of all validation supervisors required by the equipment usage of switching devices in the memory. In addition, aAPSO has been incorporated into real time application to permit a memory design based on full self-rule. Therefore, compared with the conventional design comprising of a switching-block and an isolated memory, this new method will prompt an imperative decrease of data searching among the memory read and write procedure. The proposed work is depicted utilizing Verilog language, synthesized and actualized utilizing Xilinx ISE suite based Field Programmable Gate Array (FPGA) devices. Synthesis results demonstrate that the proposed configuration accomplishes higher efficiency than the previous executions by decreasing area while keeping up a moderate throughput/Look Up Table (LUT) ratio. The proposed configuration is additionally more productive as far as power utilization.*

Keywords--- *MTCAM- Memory, Absolute Path Search Optimization, Memristive-ternary Content Addressable Memory, Low Latency and Low Power.*

I. INTRODUCTION

In the biological neural systems, synaptic weight representing the correlation between two neurons can be gradually strengthened or weakened by the ionic flow. This phenomenon seems similar with memristor's behaviour. Here memristor's conductance can be adjusted by the history of charge and flux through the memristor. These memristors that represent the nanoscale synaptic connections between the sending neurons (preneurons) and receiving neurons (post-neurons) can be structured as a crossbar array. This crossbar can be useful in realizing high density and power efficient neuromorphic architecture. In this section, the TCAM design is extended to MTCAM operation and compared with the cell of; a MCAM cell stores data ('0' and '1'), and searches (for '0', and '1') to perform a match/no-match operation. Ternary Content Addressable Memories (TCAMs) circuits are broadly utilized in location arrangements and packet filtering in networking applications. Elite Network Routers and the directing tables require enhanced look up execution quick and high capacity TCAMs.

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This segment presents a TCAM that utilizes memristors as a storage component. Regularly two memristors are associated in an arrangement to execute the task in customary memory and appropriate functions. This memory cell is quick and productively trims information and the memristors are broke down by different perspectives. The proposed APSO optimization based MeTCAM is simulated using Xilinx software.In the proposed system Each TCAM row stores one pattern of the highly frequent input operands and use a 6-transistor/2-memristor structure for each bit for the TCAM design.

II. LITERATURE SURVEY

For a few programs, the cache hit rate is enhanced to expanding the number of approaches to two way or four way cache [1], the past four way cache isn't noteworthy. More ways infer more simultaneous look-ups per getting to prompting more vitality per getting to a direct mapped cache utilizes just 30% of the vitality for each entrance as a four-way set related cache [2]. Most elevated conceivable associativity is required in execution decided applications. A novel configurable cache design [3] fuses three configurable cache parameters, these are arranged on setting a couple of bits in the setup register.

The cache can be designed in programming as either coordinate mapped, two-way or four-way set related while using the full limit of cache. Such a setup is achieved by utilizing a system called way link [4-6]. The method called line link [7] is utilized to design the cache line measure. A few designs for decreasing the vitality utilization in the cache are accounted for in the writing.

One of them is the dividing of the cache into a few little caches [8-10]. This outcome in the decrease of access time and the power cost per access. Another approach, filter cache [11] exchanges execution for control utilization by the filtration of cache references through a unusually little L1 cache. An L2 cache comparative in structure and size to an L1 cache is set after the filter cache for limiting the execution trouble. A particular option, specific cache ways in [12-14] renders the capacity to disable a subset of routes in a set affiliated cache among the intervals of modest cache action through the entire cache is operational for cache escalated periods.

In another approach, the regular unified data cache can be supplanted with multi particular caches. Everyone handles a distinctive sort of memory references according to their particular area qualities [15]. These selections make it conceivable to enhance as far as execution and power effectiveness[16].

III. PROPOSED METHODOLOGY

In a READ operation, WL = 1, and so M5 and M6 transistors arein ON condition. Both the BL and BLB bits lines are pre-charged to logic 1.

Values stored in Q and QB are transferred to the bit lines by leaving BL to its pre-charged value and at the same time discharging BLB to logic 0. Assuming that the voltage falls on transistors are negligible, the maximum voltage applied to M1 or M2, V_{Write}, must satisfy the following equation (1).

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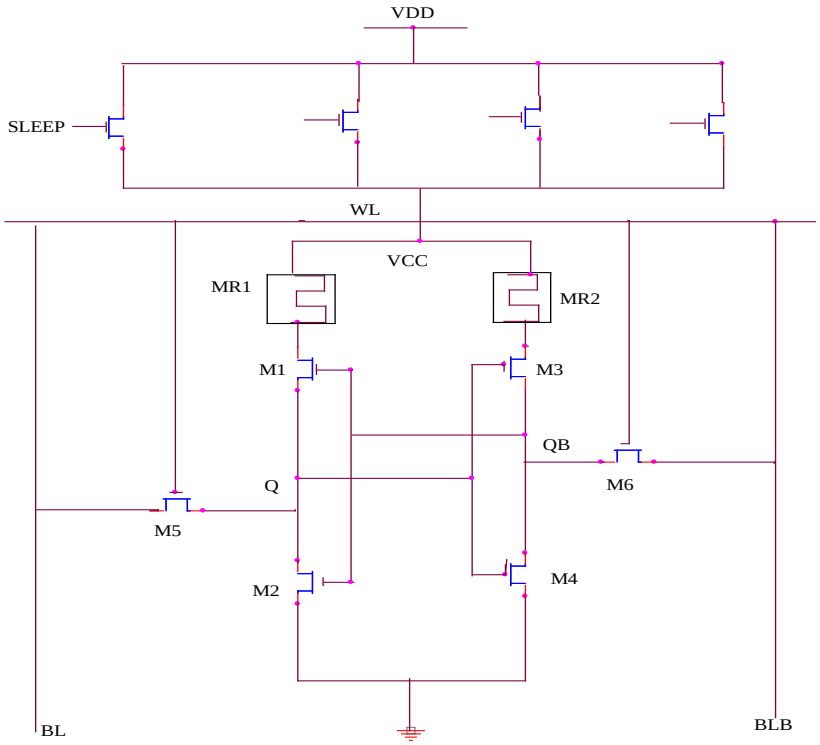

Figure 1: APSO Technique employed 6T-2M Memristor based SRAM

$$Vwrite > V_{SET} \text{ and } V_{RESET} \quad (1)$$

Hence the proposed work minimizes this leakage current,with the technique of sleep which considers high threshold voltage transistor that can be nMOS.

3.1. Absolute Path Search Optimization (APSO) Algorithm

Among write task, if there is a hit from anyway, at that point the set relating to that specific way will be chosen with the assistance of list.

Pseudo Code of write mode:

Input: Write Sequence Ws (Match Line sensing)

Output: Stored Pattern Set Ps.0, 1, x

Start

Write the bit of sequence Bs.

Bs = $\int size(Ws)$

For each cell Ci from Bs

Store the Pattern Si.

Si = $\int_{i=1}^{Bs} Subset(Ws, Ci)$

Add to pattern set Ci.

Ci = $\sum_{i=0}^{n} W(0) \in W(1)) \cup Bs$

End

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If pattern Ci = '1' then

Send single block write command

Else

Send multi-block write command

End if

If received response = 'True' then

Go to decision process

Else

Stop.

While reading the cache all the four different ways will be empowered. The set, from where the information must be read, is chosen, with the assistance of list bits separated from the address bits originating from the processor.

Input: Cell Pattern Set Ps, Pattern Pi (Search line sensing)

Output: Search word or sequence. S_{Out}

Start

Step 1: Put on search key.

Step 2: Distribute search key into N substitute words.

Step 3: Entirely layers custom algorithm 1 in parallel. S

Step 4: Get Match Address (MA) among Potential Match Address (PMAs) /divergence occurs

Step 5: If all PMAs authenticate their consistent sub words

For each cell l from Ps

Step 6: Calculate similarity.

$$S_{Out}=\int_{i=1}^{cells} \int_{j=1}^{size\,(Ps)} \sum Ps(j,l) == Pi$$

Where i = Number of Memory Bits

j = total size data

Step 7: $S1out = \frac{Sout}{size\,(cells)}$

Step 8: Else

Mismatch occurs

End If

Stop

IV. SIMULATION RESULTS

This section discusses the simulation results and performance analysis of the proposed APSO based MeTCAM. The performance of the proposed MeTCAM system is validated through simulation using Xilinx14. The following figure and tables show the simulation results and performance analysis of the proposed system.

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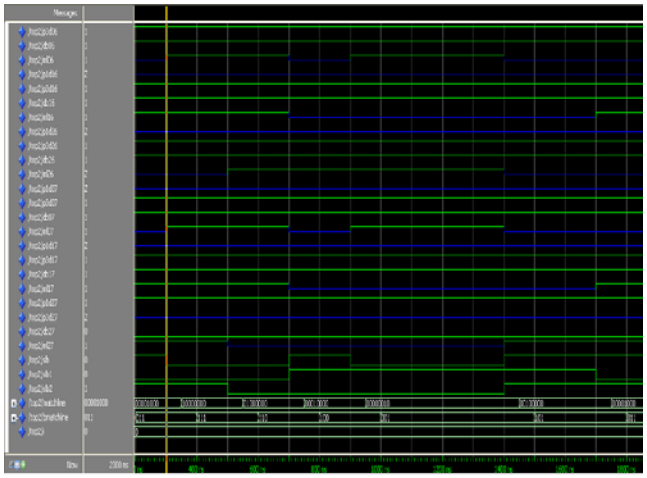

Figure 1: Matched results of MeTCAM

The data search operation of the proposed deep search pattern based MeTCAM simulation result are shown in Figure.3. This simulation result clearly demonstrates that the searched data are available inside the MeTCAM cells and marked in blue lines.

Figure 4 represents the average current, peak current, average power and peak power consumption of the proposed

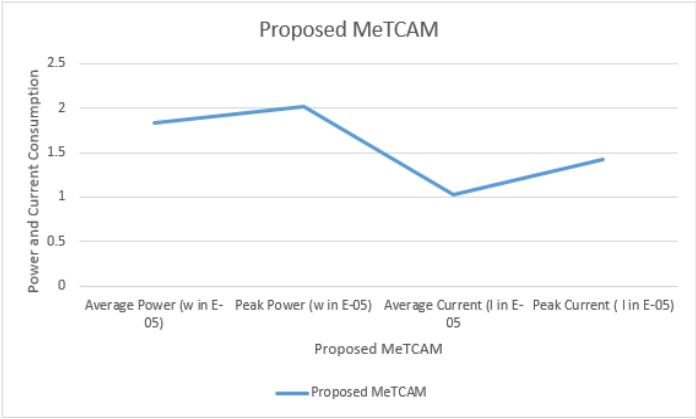

Figure 2: Power and Current Consumption Analysis

APSO Method based MeTCAM system. By using APSO Method, the overall response of the current and power consumption is low.

V. CONCLUSION

This section proposes a hybrid structure for a ternary CAM (TCAM) that utilizes two Transistors and memristors to defeat all issues. The proposed TCAM memory cell is researched concerning a few features, such as resistance and voltage range of the memristor. A farreaching simulationbased assessment of this TCAM is developed using Xilinx programming language utilizing APSO Method. The Simulation work exhibits that the execution of the

proposed algorithms is better than the past methods for improving the performance of search applications**.** An Overall efficiency of 97.5% was achieved by using this proposed system.

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