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16QAM Wireless Communication Model

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A. Abstract--- *Software defined radio (SDR) has emerged as a priority theme of research since it will substitute for conventional implementation on wireless communication system. In this paper, a multi-standards SDR model is designed and implemented in FPGA form using Xilinx system generator technique. According to the under sampling theory which is used in this model, the received 70MHz carrier is sampled at 40MHz and the performance of the proposed model with different standards' like GSM,OFDM, and WCDMA using 16QAM modem is produced attractive behavior with different channel effective and minimum BER. Therefore make develop on 3G of wireless and mobile systems more economical, effective and accelerate the transition from 3G to 4G of wireless systems.*

Keywords: *SDR, FPGA, Wireless Communications.*

I. INTRODUCTION

Field-programmable gate arrays (FPGAs) are widely used to implement physical layer signal processing functions for software-defined radios (SDRs [1] [2]). FPGAs provide very high performance custom hardware solutions, and can be reconfigured in system, and when bringing up a new waveform in the modem. Despite their reprogrammability, they have historically been considered part of the "hardware" within a modem, rather than part of the "software". Consequently, the SDR software control layer, or Software communications Architecture (SCA [3]), has largely ignored issues related to the specification, configuration, signal transport, or inter-component interfaces thatare important to the platform provider of an SDR that exploits FPGAs. Wireless communication networks have become more popular in the past two decades since the advent of cellular communications. The rapid growth in cellular communications has proved that wireless communication is viable for voice and data services. Traditional wireless devices are designed to deliver a single communication service using a particular standard [4]. With the steady increase of new wireless services and standards, single purpose devices with dedicated hardware resources can no longer meet the user's needs. It is also expensive to upgrade and maintain a wireless system each time a new standard comes into existence. A feasible solution to make communication systems more flexible and user friendly can be achieved through the software defined radio (SDR) concept. Software defined radio refers to the class of reprogrammable or reconfigurable radios in which the same piece of hardware can perform different functions at different times [5].

II. SYSTEM MODEL FOR IMPLEMENTATION

Simulation of the SDR system with SIMULINK tools forms is the first step of the design process for reconfigurable computing. For an exact representation of the FPGA implementation, the Xilinx system generator block set in MATLAB is used. The complete simulink SDR model show in Fig (1) and the parameters of proposal model are given in table (1).

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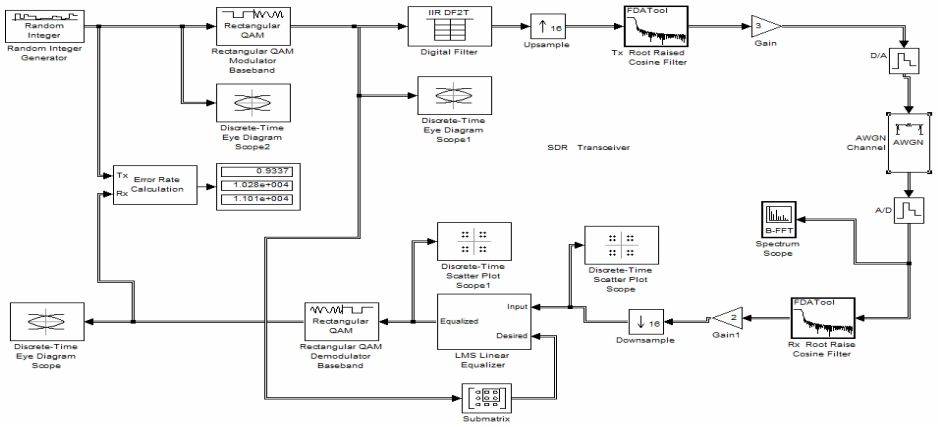

Figure 1: proposed SDR transceiver model.

Table 1: Simulation Parameters of Proposed Model

Modulation Type	16QAM
Symbol Rate	2.5Msymbol/Second
Interpolation Factor	16
Channel Model	AWGN
Receiver Sampling Rate	40 MHz
IF	70MHz

III. SYSTEM GENERATOR BASED DESIGN FLOW

Simulation and testing of the transceiver design flow were done using *System Generator*, a system level modeling tool from Xilinx [6]. This tool can be used for designing and testing DSP systems for FPGAs in a visual data flow environment such as MATLAB *Simulink*. The *System Generator* based design flow [7] is shown figure (2). The system model is created in the MATLAB environment using Xilinxlibrary. This diagram shows one of three ways to design a system. This is a typical design flow for HDL Co-Simulation. This diagram shows that we can use Black Box and include user's VHDL code or IP core along with Xilinx System Generator's blocks in the design and generate a synthesizable design which can be implemented using Xilinx ISE's Project Navigator. It also uses ModelSim block which is a helper block to invoke ModelSim simulator and actually simulate the design. The simulator's output is fed back to Simulink and the results can be displayed using Simulink'ssinks.

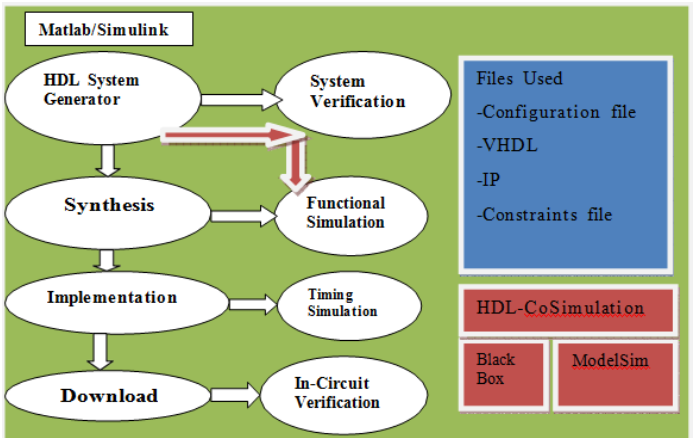

Figure 2: System Generator based design flow (Xilinx Inc., 2003).

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System Generator Design

The goal of our implementation is to mimic an ideal SDR based 16QAM communication system. Quadrature Amplitude Modulation, QAM, has fast become the dominant modulation mechanism for high speed digital signals. From the wireless 802.11 protocols to ADSL modems to personal communicators for the military, QAM has become a necessary part of our daily lives. With increases in processing power, QAM as a part of software defined radio (SDR) schema is now easily achievable. This section details a System generator implementation of 16-QAM communication system in FPGA which would be suitable for a SDR system. Figure (3) shows a high level SDR transceiver.

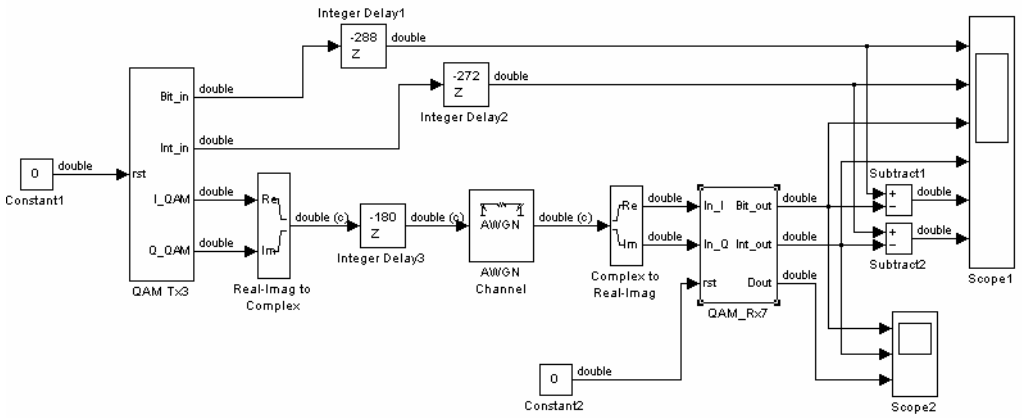

Figure 3: 16-QAM transceiver using system generator

The implementation can be broken down into three main stages: transmitter, channel and receiver. The modulation and demodulation stages are comprised of several distinct subsystems.

4.1. Transmitter

In the transmitter, the baseband signal is generated using programmable digital signal processing techniques. The generated signal is 16QAM with a symbol rate *2.5Msymbole/sec.* The transmitter part show in figure (4) and the constellation -eye diagram of the generated baseband signal show in fig.(5).

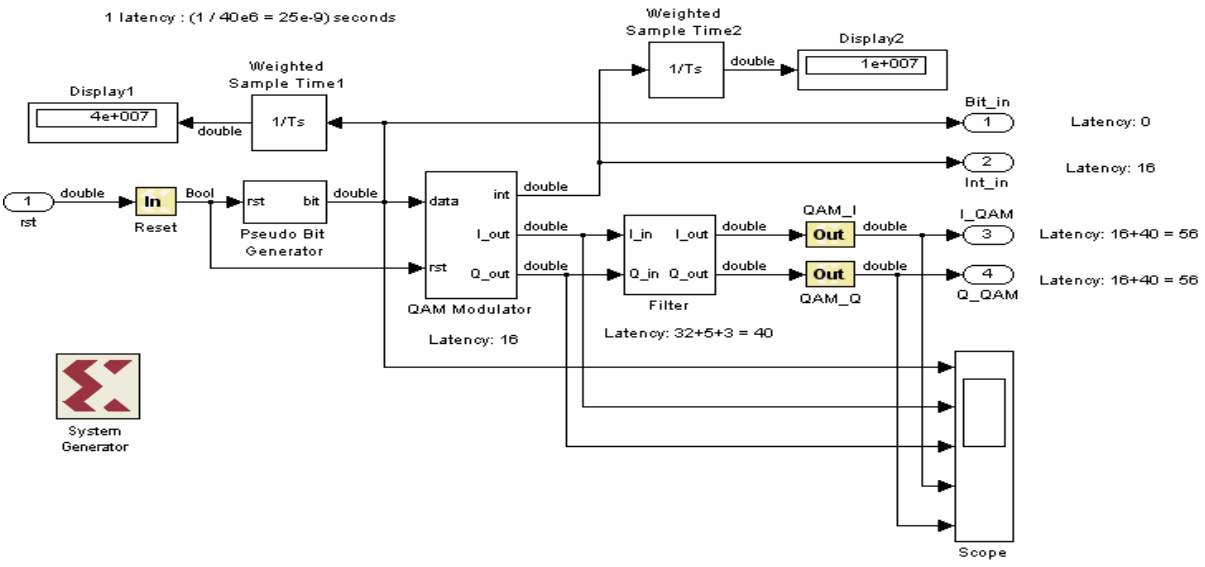

Figure 4: 16-QAM Transmitter (QAM Tx3 subsystem) using System Generator.

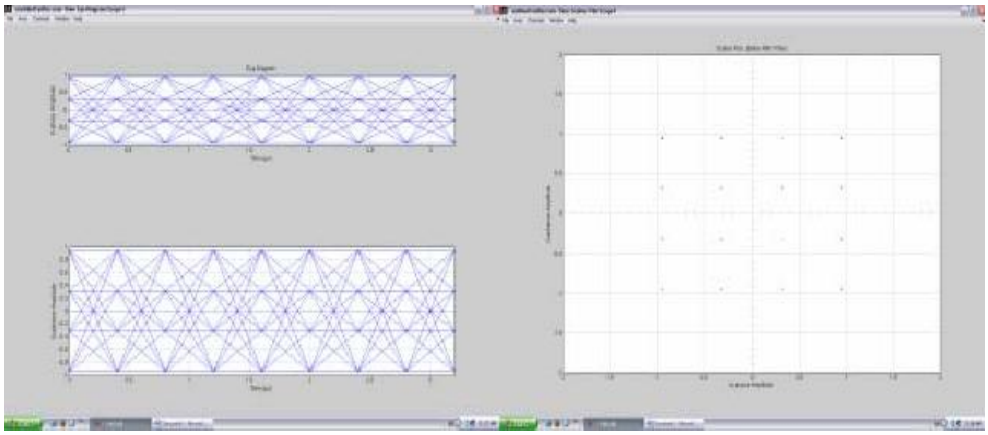

Figure 5: Generated Baseband Signal: (a) eye diagram, (b) constellation diagram.

The input and output signals for transmitter part is show in figure (6). As show from signals the input bit of 10Mbps was modulated first and transferred to 2.5Msps 16QAM baseband (IQ) signal. The signal is then passed through a channel distortion filter to show the effect of ISI in the system. After that, the signal is passed through pulse shaping filter (root raised cosin filter) to limit the transmitted bandwidth. Finally, it is up-converted to IF using NCO (Numerically Controlled Oscillator). The final stage is the IF-to-RF conversion which is typically implemented in the analog domain.

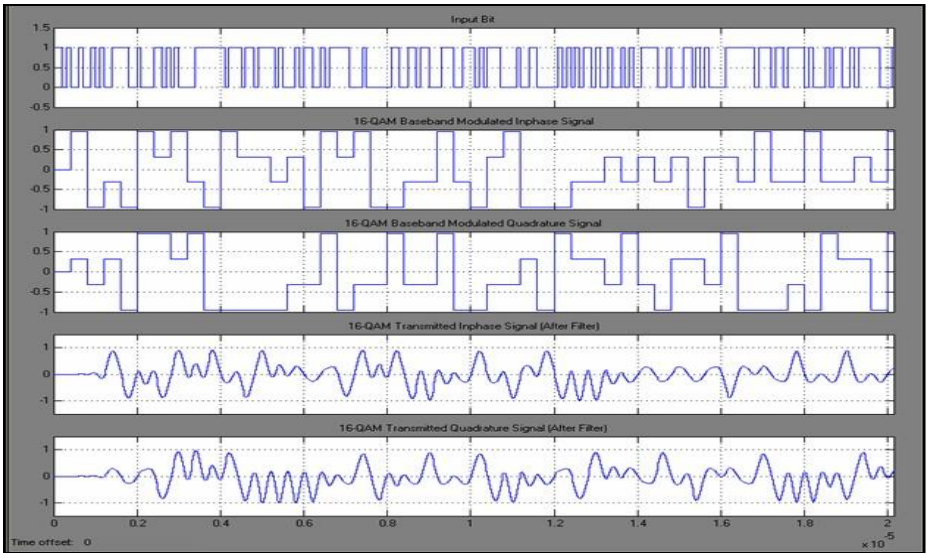

Figure 6: Transmitted Signal: Input bit = 10 Mbps, (16-QAM Baseband Modulated (IQ) signal = 2.5Msps), (16-QAM Transmitted (IQ) signal =16*2.5 = 40 Msps (16 bit, 13 fractional length).

4.2. Channel

The transmission channel has several effects on the signal in a physical system. The finite bandwidth of the channel will cause distortion in the ideal signal, noise from various sources will also be introduced and finally the channel may also attenuate the input signal. Other effects, such as dispersion, may also be present. The effects of attenuation and noise can be modelled by adding Gaussian white noise to the signal, effectively changing the signal to noise ratio present at the receiver. The effects of finite bandwidth can be modelled by a simple filter. The original power spectrum of baseband transmitted signal is show infig.(7).

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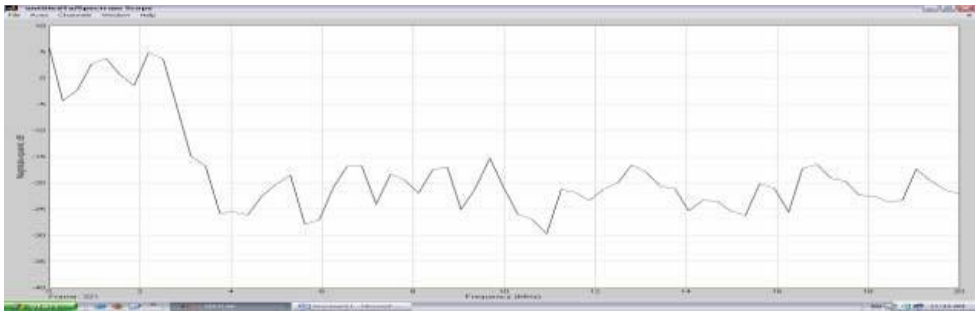

Figure 7: power Spectrum of Original Baseband Signal.

4.3. Receiver

In the receiver, after the signal is contaminated by noise, it down converted to IF and then sampled and processed using programmable digital signal processing techniques. The IF input signal is at 70MHz while the sampling frequency used in the proposed receiver model is 40MHz so, under-sampling technique plays the main role in the receiver stage. A fundamental part of many communication systems is the digital down converter. This allows a signal to be shifted from its carrier (or IF) frequency down to baseband. The sampled IF signal is down converted to its baseband through a digital down converter (DDC) works by first shifting the bandwidth of interest to baseband by multiplying the received signal by a close approximation to the original carrier. This work is based on the simplified mathematical principle. There is a technique known as bandpass sampling used to sample a continuous bandpass signal that is centered about some frequency other than zero HZ. When a continuous input signal's bandwidth and center frequency permit us to do so, bandpass sampling not only reduces the speed requirement of A/D converters below that necessary with traditional low-pass sampling; it also reduces the amount of digital memory necessary to capture a given time interval of a continuous signal.The demodulation section is by far the most complicated part of the QAM model. The demodulator must detect the phase and amplitude of the signal, decode the symbol based on the phase and amplitude and then finally convert the data back to a serial stream. In order to complete the symbol demodulation, recovery of the symbol clock is required. Figure (8) shows the receiver system generator block. The constellation and eye diagram of received baseband 16QAM signal is show in fig.(9).

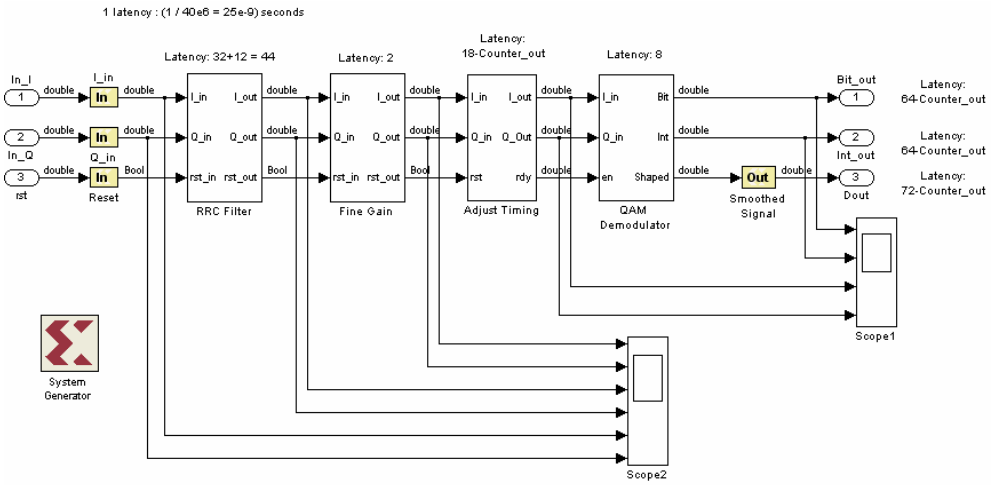

Figure 8: Receiver part of 16-QAM (QAM Rx7 subsystem) using System Generator.

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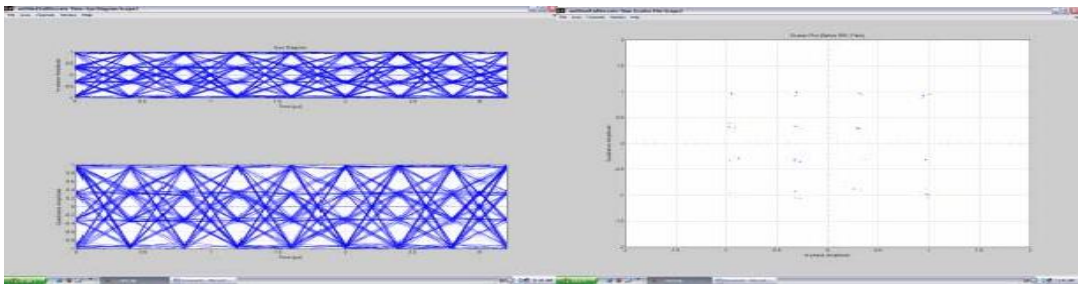

Figure 9: 16QAM baseband received signal: (a) eye diagram, (b) constellation diagram.

It is obvious from eye diagram the effect of inter-symbol interference as the eye is nearly closed. And from the constellation diagram, the received signal suffers from phase error due to noise and channel distortion. In order to solve this problem, an adaptive equalizer (variable taps coefficients using LMS Algorithm) is used to improve the system performance and reduce the error in phase. This is clearly shown in Fig.(10) which represents the constellation diagram of signal before and after equalization.

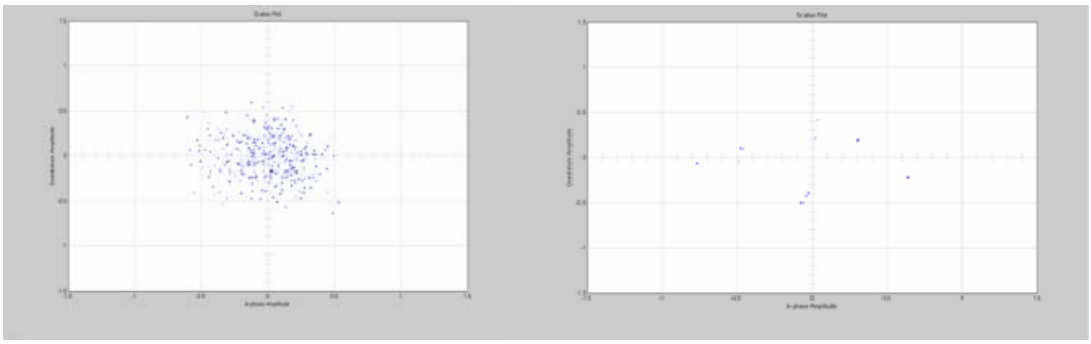

Figure 10: Constellation diagram of the received baseband signal (a) before equalizer, (b) after Equalization.

The input and output signals for receiver part is show in figure (11),(12).

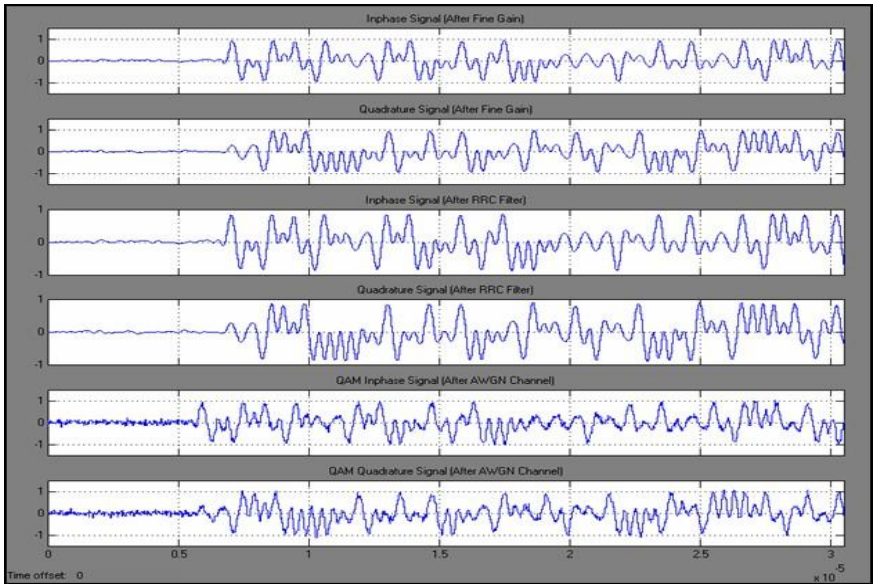

Figure 11: Receiver Signal

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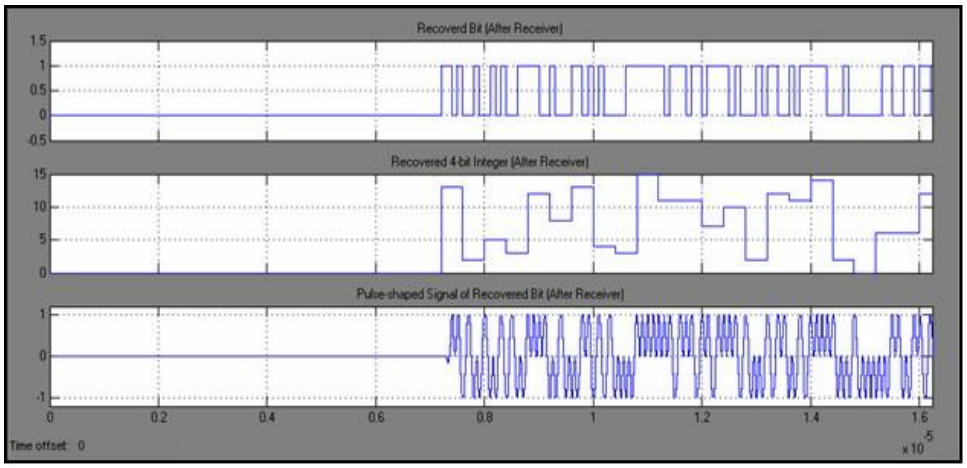

Figure 12: Receiver Output Signal: Recovered 4-bit Integer =5 Msps, Recovered bit: 2.5*4 = 10 Mbps, Pulse-shaped signal of Recovered bit: 10*8 = 80 Msps (16 bit, 14 fractional length).

4.4. Timing Recovery

In any QAM scheme timing recovery poses a significant problem for the recovery of a quality signal. A wide variety of methods are available for timing recovery, however, their usefulness actually depends on the type of transmitted data. The simulation software will be using a Bernoulli coded random bit sequence so none of the decision based schemes would have an advantage. In this case the best choice would be a synchroniser timing recovery circuit. To reduce complexity, a simple times-two timing recovery system was implemented. After a significant amount of tuning, the timing recovery still had a significant amount of jitter. As expected, the jitter was dependent on the data being transmitted. Directed timing recovery as the best recovery scheme for random signals as show in fig(13).

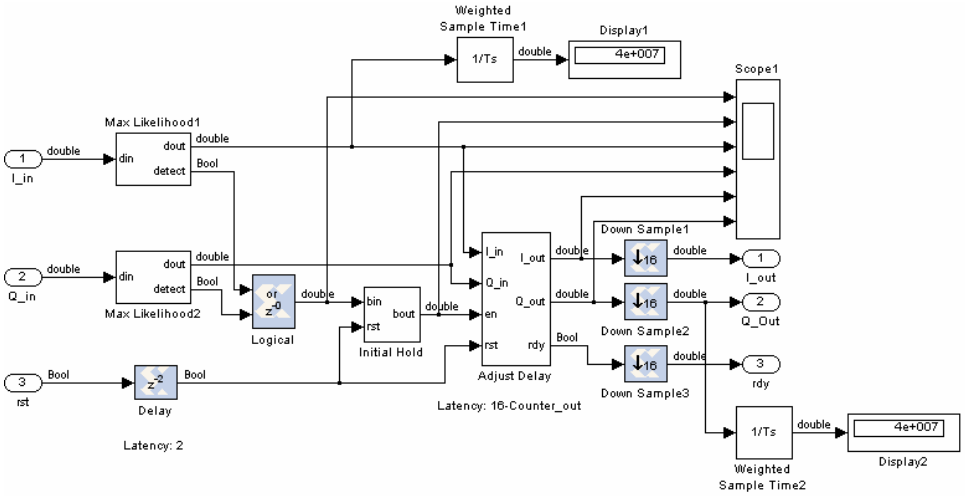

Figure 13: Timing Recovery (Adjust Timing subsystem in QAM Rx7)

4.5. FPGA Implementation Results

The final step in our design is to download the system generator model HDL cod to the FPGA form Virtex-4 using Xilinx system generator program. In this paper the transmitter part of the SDR system is implemented in FPGA Virtex-4 board number (1) using the HDL code of system generator, which is used to analyze the system. The

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receiver part of SDR system is implemented in FPGA Virtex-4 board number (2).Fig.(14) show the Physical Assembly of SDR transceiver.

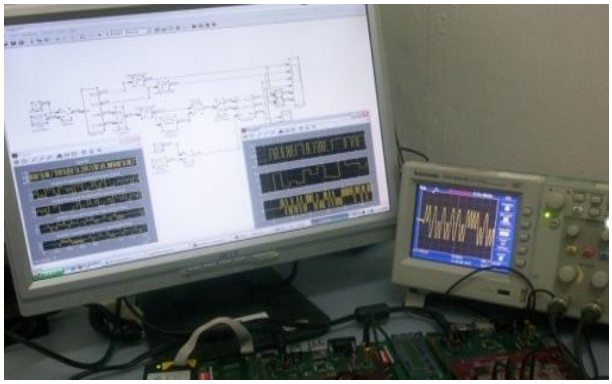

Figure 14: Physical Assembly of SDR transceiver

The details of transmit and received IQ signal is show in figs.(15),(16) and (17).

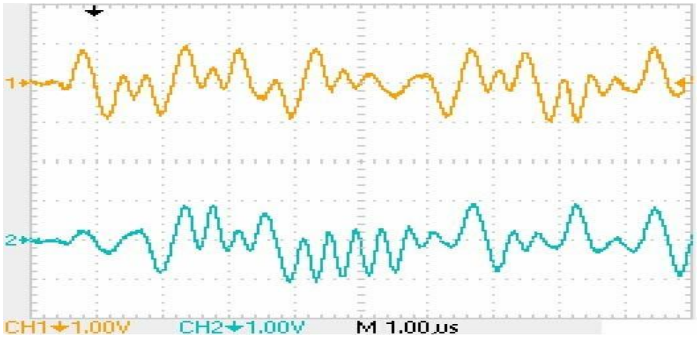

Figure 15: transmitted (IQ) QAM signals fromDAC

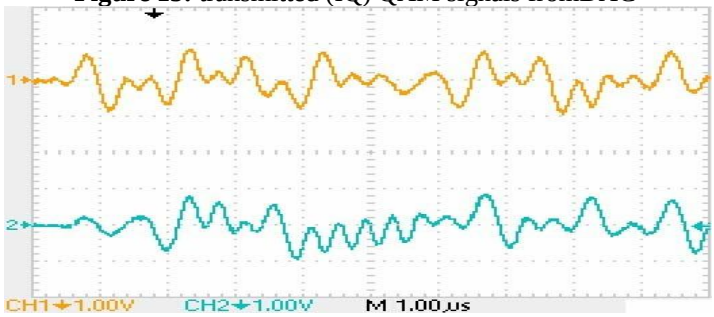

Figure 16: receiver IQ signal Filtered by RRCfilter.

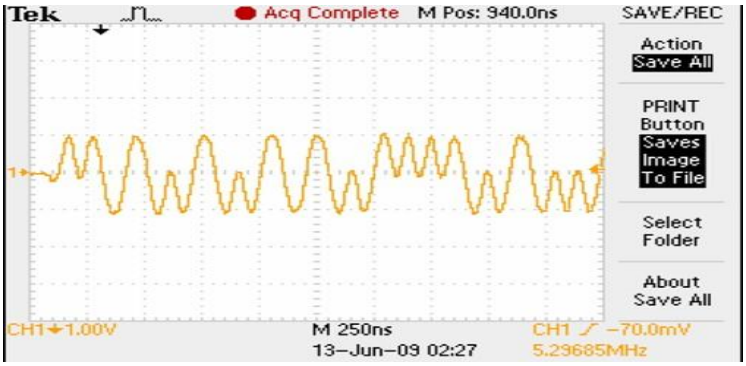

Figure 17: output signal of receiver FPGA after DAC.

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IV. CONCLUSION

In this paper the design of Software Defined Radio (SDR) model is present. For the design of SDR model in Matlab/Simulink, the transmitted signal with 2.5 MHz bandwidth undergoes 20 dB SNR (Signal-to-Noise Ratio) in Additive White Gaussian Noise (AWGN) channel between transmitter and receiver. The similarity of demodulated output data in receiver and input data of transmitter in integers (10 Mbps) shows the communication between transmitter and receiver is successful, although bit (data) error may occur. For the design of SDR model in System Generator, Pseudo Noise Generator module is used to generate 10 Mbps random bits as transmitter input data. In receiver part, Adjust Timing module is required to recover symbol timing for optimum sampling point for the following demodulation process. The demodulated output data in receiver is pulse-shaping of the reconstructed bits because 50 ohm transmission line transformer after DAC in P240 Analog Module does not allow DC (direct current) signal to flow through it, despite the demodulated output is reconstructed bit in ideal case of receiver in SDR model. However, the AWGN channel is also 20 dB SNR for 2.5 MHz bandwidth signal transmission between transmitter and receiver. Both the real-time (empirical) and simulated results for transmitted signal and receiver output in time domain shows equivalence in shape although there are some minor differences due to limitation of the 50 ohm transmission line transformer after DAC in P240 Analog Module. The equivalence also proves the bit-true and cycle- true of the FPGA processing which are important in high speed DSP for further processing of pre- coding, decoding and equalization in more advanced SDR model. Therefore this develop on 3G of wireless and mobile systems more economical, effective and accelerate the transition from 3G to 4G of wirelesssystems.

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